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MT6236 Design Notice V0.2

2010/10

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Revision History

Rev.	Date	Author	Description
V0.1	2010.07.14	Hank Chang	First version release
V0.2	2010.10.13	Hank Chang	**Design Notice** 1. Add notice of current sink for backlight, flashlight driver 2. Modify PMU power on sequence 3. Update pulse charger design notice 4. Add notice for 2-on-1 speaker application 5. Update camera power design notice : (1) Config VCAMA=2V8 and connect to DVDD_CAM (pin Y19) and Camera DOVDD and Camera AF power (2) Config VCAMD=1V5 and connect to Camera DVDD (3) Add external LDO (250mA, PSRR=VCAMA) for Camera AVDD (4) Add bead (600@100M) on above three camera power source 6. Add Audio bead selection guide 7. Update High Speed Memory Layout Rule(DDR) **Layout Notice** 1. Add Priority for Layout Placement / Routing 2. Modify PCB Layout Design Notice and add Dual Camera Notice 3. Add FM De-Sense Layout Guide **Issue Case Study** 1. Add Issue Case Study - 1 : MSDC IOT issue 2. Add Issue Case Study - 2 : EINT 7~9 MUX issue

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Outline

- MT6236 Features Overview & Package
- Major hardware difference between MT6236 & MT6235
- Design Notice
  - PMU
  - Pulse Charging
  - Bluetooth
  - USB
  - Audio/Speech
  - GPIO Selection
  - ADC/TP
  - External Memory Interface
  - Camera
  - De-sense
  - Tool Version
- Layout Notice
- Issue Case Study
- Appendix:
  - MT6236 High Speed Memory Layout Rule(DDR)
  - MT5921 Application Note for MT6236

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MT6236 Features Overview

Edge Platform: MT6236 + MT6140/AD6548

Target Market: **EDGE phone** with 312MHz CPU clock/Advanced UI/Up to 5M Camera with enhanced user-experience functions/Rich S/W Multimedia/BT

Features:

- ARM926EJ-S **312 MHz** with cache
- PMU/Touch panel driver integrated
- Bluetooth 2.1 integrated
- Class-D Amps(900mW) integrated
- 5Mp ISP integrated with advanced features
- FR, EFR, HR, AMR speech codec
- Supports up to HVGA LCM
- Supports various melody formats
  - MIDI, WB AMR, AAC, AAC+, eAAC, digital music
- Polyphonic melody, 64-tone wave table, stereo loudspeaker
- SBC encoder capability with Bluetooth A2DP function
- Advanced DSP acoustic functionality
  - AEC and noise reduction
- Supports QWERTY keypad
- Multi-memory system with more flexibility for phone design, which supports
  - NOR/pSRAM with AD MUX; with burst mode (up to 104 MHz)
  - NAND-boot
  - NAND data storage
  - LPDDR SDRAM
- Supports SD, MMC, Memory Stick, Memory Stick Pro, SDIO cards
- Supports dual SIM
- Built-in USB 2.0 (High-speed/Device), IrDA
- Package size: 12.5x12.5 mm^2 ,382 balls TFBGA with 0.5 mm pitch

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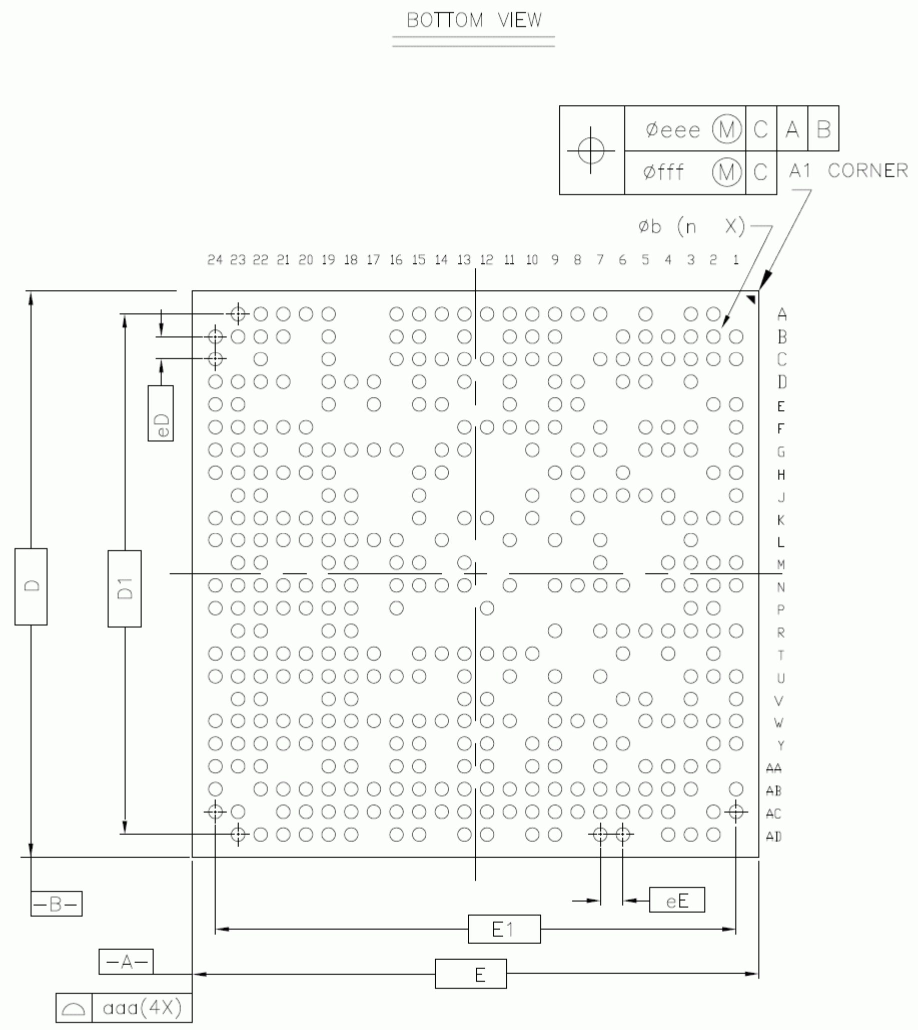
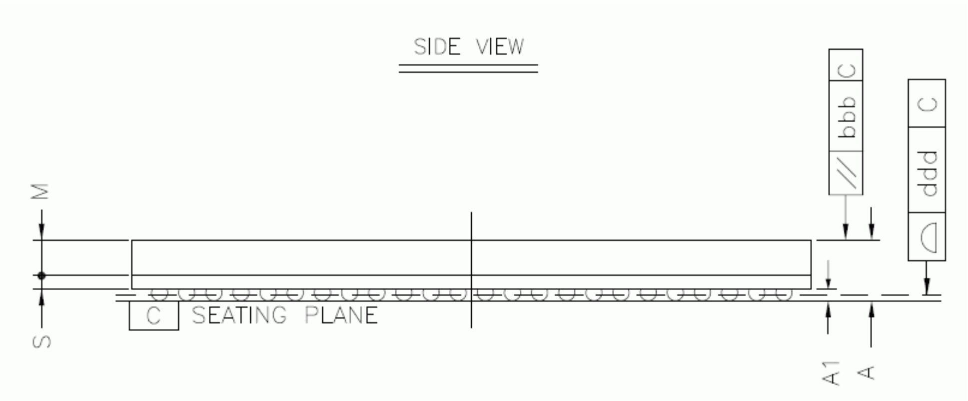
MT6236 Package





Package	Body Size		Ball Count	Ball Pitch		Ball Width	Total Thickness	Stand Off	Mold Thickness	Substrate Thickness
	D	E	n	eE	eD	b	A (Max.)	A1	M	S
TFBGA	12.5	12.5	382	0.5	0.5	0.27~ 0.37	1.2	0.16~ 0.26	0.65	0.26

Major HW difference between MT6236 & MT6235

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Function		MT6235	MT6236	Refer to section of MT6236 Design Notice
Package		13x13mm^2, TFBGA/362 ball	12.5x12.5mm^2, TFBGA/382 ball	Package
GPIO pins (Power domain & MUX)		75 GPIOs	67 GPIOs	GPIO selection
Share-pad		No share-pad	(1) USB_DP/DM & UART1 TX/RX (2) CMDAT[0:5] & MIPI interface (RDP[0:1], RDN[0:1], RCP, RCN)	USB GPIO selection
Bluetooth		Not integrated	Integrated	Bluetooth
Camera MIPI interface		Not support	Support	GPIO, Camera
Memory support		1. NAND+SDR 2. NOR+PSRAM(ADDMUX)	1. NAND+DDR 2. ADMUX NOR+PSRAM	External Memory Interface
Audio	Internal audio amp	Not integraed	Integrated one class-D amp (900mW@4.2V)	Audio

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Major HW difference between MT6236 & MT6235

Function		MT6235	MT6236	Refer to section of MT6236 Design Notice
PMU	General	X	Fold-back current limit	PMU
PMU	LDO (besides VCORE/VM/VRF/VCAMA)	Need near-end & far-end bypass cap	Need only far-end bypass cap	PMU
PMU	LDO	Vout & Imax	Vout & Imax	PMU
PMU	Buck	1 Buck : Vcore	2 Buck : Vcore & Vm	PMU
PMU	LCM backlight	Not integrated	Integrated 1. Boost controller for Serial LCM back-light 2. Driver for Parallel LCM backlight	PMU
PMU	LED_KP VIBRATOR	Open Drain N-MOS : LED_KP:150mA VIBRATOR:50mA	Open Drain N-MOS : LED_KP:150mA (8steps) VIBRATOR : LDO mode (200mA)	PMU
Charger		Linear charger	Pulse charger	Ch

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Design Notice - PMU

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Content

- MT6236 Introduction
  - General description
  - Block diagram
  - Buck/Boost/LDO list
- Comparison
- Function Description
- Reference design
- Appendix

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MT6236 Introduction – General description

- The MT6236 is built-in high performance power management IC.
- Highly integrated functions fulfill all power requirement in handset system
  - Buck converter * 2
  - LDO
    - Analog LDO * 4
    - Digital LDO * 9
  - Audio Amplifier
    - Class-D 0.9W@4.2V * 1
  - Charger controller
    - AC/USB
    - Pulse-Charger
  - Boost controller
    - Serial LCM back-light LED 6
  - Driver
    - Parallel LCM backlight LED 5
    - Keypad back-light * 1

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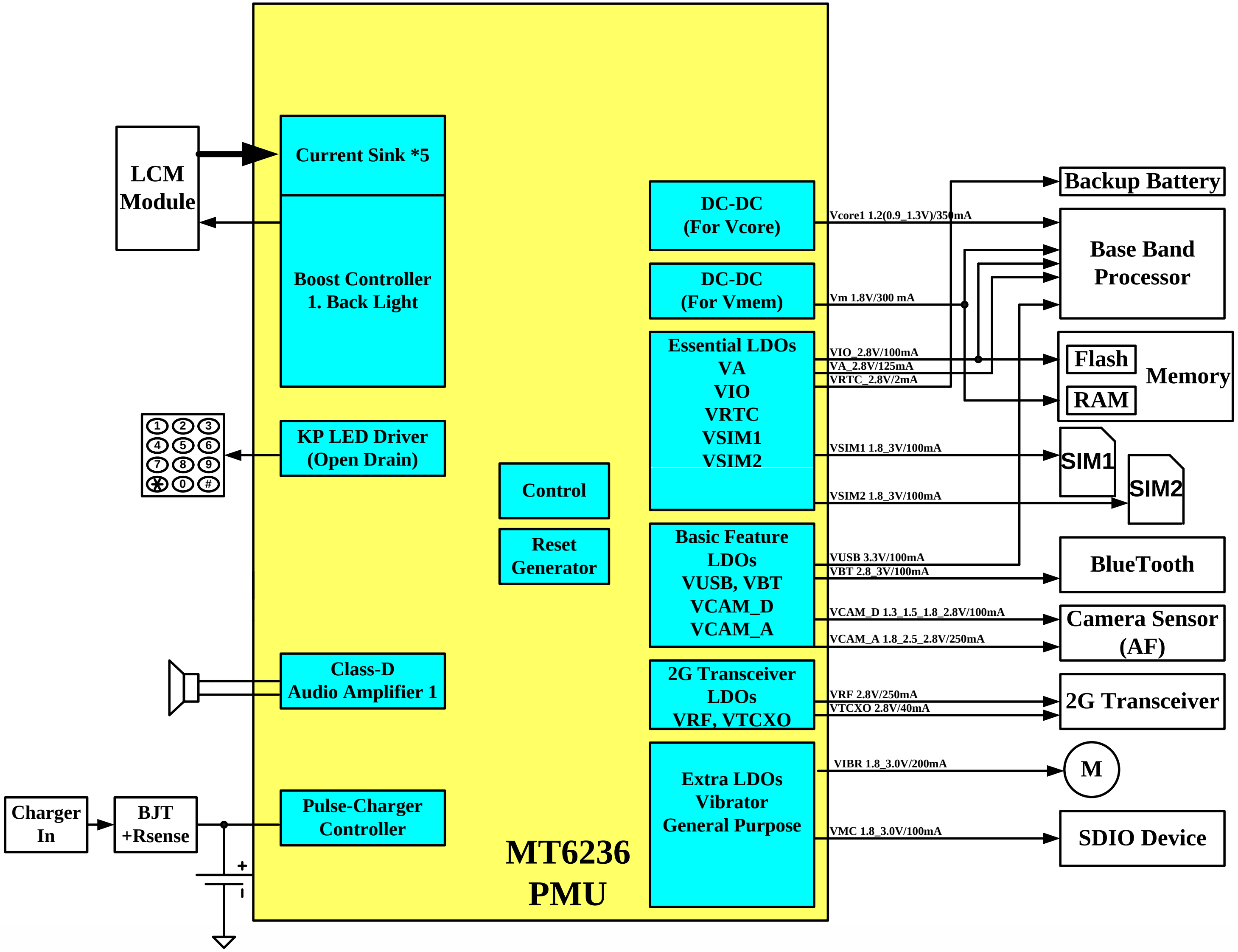
MT6236 Introduction – Block Diagram



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MT6236 LDO List

Vcore/VM/VRF/VCAMA need near-end bypass cap

Regulator	Output Voltage (V)	Output Current (mA)	Output Components	Notes
VCORE	**0.9~1.3**	350	2.2uH + 4.7uF	Max. output current = 100mA when set to < 1V
VM	1.8	300	2.2uH + 4.7uF	
VRF	2.8	250	2.2uF	
VCAMA	1.5/1.8/2.5/2.8	250	2.2uF	
VA	2.8	125	1uF/0.1uF	Far-end bypass cap
VTCXO	2.8	40	1uF	Far-end bypass cap
VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	1uF*2	Far-end bypass cap
VIO	2.8	100	1uF	Far-end bypass cap
VBT	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	1uF	Far-end bypass cap
VUSB	3.3	100	1uF	Far-end bypass cap
VSIM	1.8/3.0	100	1uF	Far-end bypass cap
VSIM2	1.3/1.5/1.8/2.5 2.8/3.0	100	1uF	Far-end bypass cap
VMC	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	1uF	Far-end bypass cap
VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1uF	Far-end bypass cap
VRTC	2.8	2	0.1uF	Backup battery

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Content

- MT6236 Introduction
- Comparison
- Function Description
- Reference design
- Appendix

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The MT6236 Comparison (1/3)

Block	Sub-block	MT6235		MT6236	
SOC		SOC		SOC (65nm)	
General	Bandgap	YES		YES	
	DDLO	2.5V		2.5V	
	UVLO	2.75V (power on) 2.9V (steady default) Configurable		2.75V (power on) 2.9V (steady default) Configurable	
	Reset	YES		YES	
	Soft-Start	YES (Default On LDOs)		YES (Default On LDOs)	
Protection	Thermal Shutdown	YES		YES	
	Fold-back Current Limit	NO		YES	
		Vout	I_max	Vout	I_max
Buck Converter	VCORE	1.2/0.9 (DC/DC)	350	1.2/0.9 (Buck + LDO Mode)	350
	VM	x (LDO mode)	x	1.8	300
		Vout	I_max	Vout	I_max
Analog LDO	VTCXO	2.8	40	2.8	40
	VA	2.8	125	2.8	125
	VCAMA	1.5/1.8/2.5/2.8	250	1.5/1.8/2.5/2.8	250
	VRF	2.8	350	2.8	250

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The MT6236 Comparison (2/3)

Block	Sub-block	MT6235		MT6236	
Digital LDO	VM	1.8	300	x (Buck mode)	x
	VIO	2.8	100	2.8	100
	VSIM	1.8/3.0	80	1.8/3.0	100
	VSIM2	1.8/3.0	20	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VUSB	3.3	75	3.3	100
	VBT	2.8/3.0	100	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VCAMD	1.5/1.8/2.5/2.8	75	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VMC	x	x	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VIBR	x	x	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200
RTC	VRTC	1.5/1.2	0.02	2.8	2
	BAT_BACKUP	2.8	2	-	-
Driver	Boost	No		20mA/21V	
	LED_KP	150mA		150mA (8 steps)	
	VIBRATOR	250mA		x (LDO mode)	
	Current Sink	x		5 x (24mA, 0.25V), Sharing (Individual Current/Enable control)	

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The MT6236 Comparison (3/3)

Block	Sub-block	MT6235	MT6236
Audio Amplifier		x	Class D (0.9W, 4.2V)
Charger	Charger type	Linear charger	Pulse chager
	Maximum Input Voltage	9	30
	Maximum Charging Voltage	7	Programmable
	OV	4.3	4.35
	CC Mode	160mV/Rsense	160mV/Rsense
	Pre-Charge Mode	100mA	50mA/100mA
	Battery Detection	V(NTC Pin)	V(NTC Pin)
	Watchdog Timer	x	Yes
SIM_LS		2	2

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Content

- MT6236 Introduction
- Comparison
- Function Description
  - Power on timing
  - Buck
  - Boost
  - Driver
  - Audio AMP
- Reference design
- Appendix

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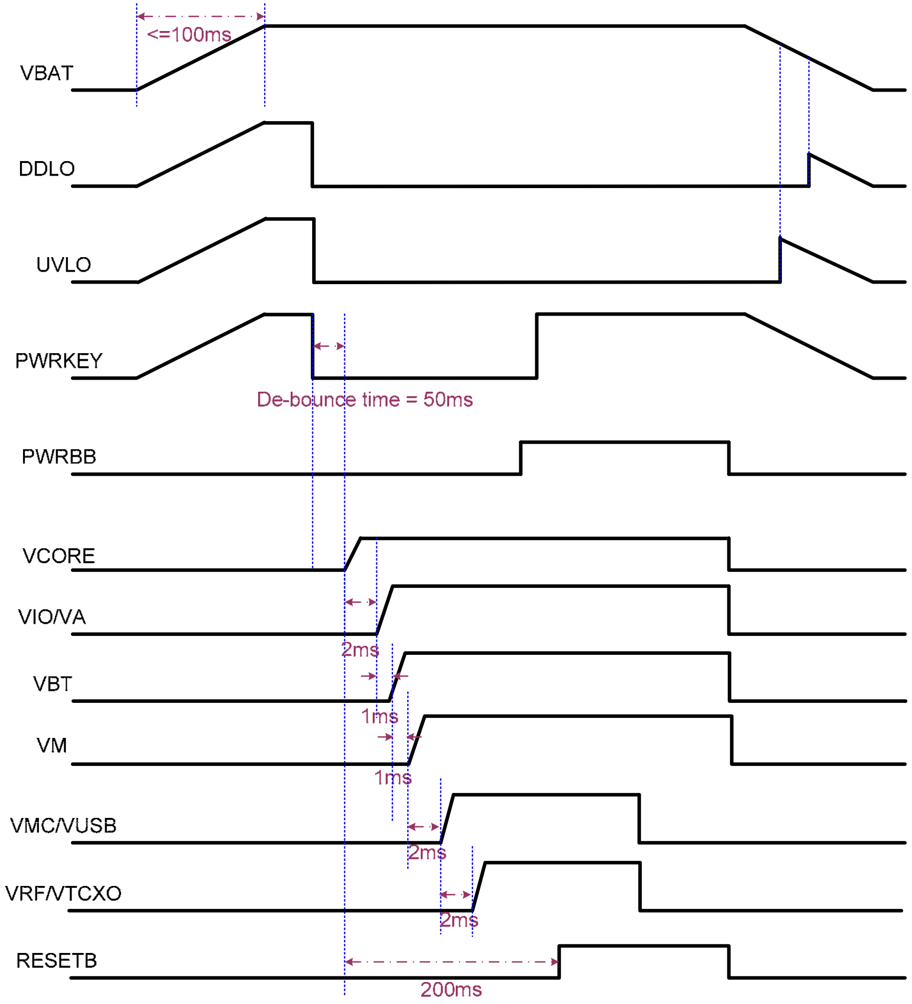
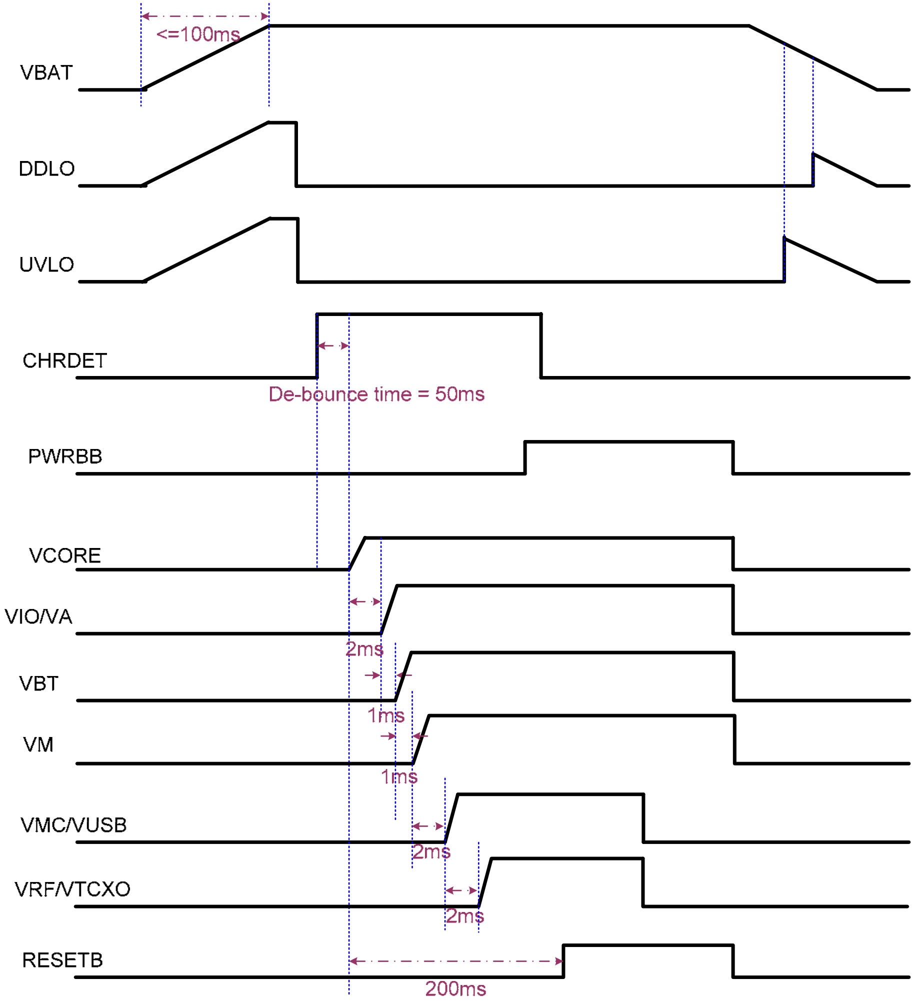
Function Description - Power On/OFF Timing Control



Press PWRKEY



Charger Plug-in

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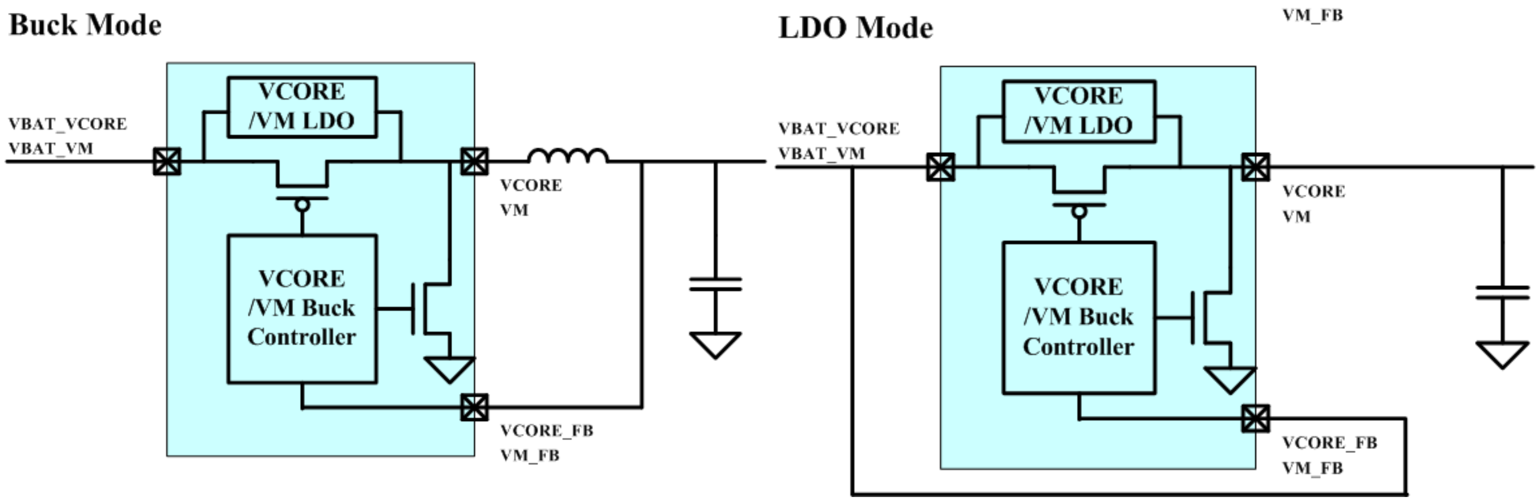
Function Description - Buck Converters With LDO Mode



- Among 2 buck converters, V_{CORE}/V_M also provide LDO mode for lower cost requirement.
  - VCORE (Buck/LDO: 350mA/300mA)
  - VM (Buck/LDO: 300mA/200mA)
- Buck mode: VCORE_FB/VM_FB connect to the output capacitor.
- LDO mode: VCORE_FB/VM_FB connect to VBAT.

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Function Description - Boost Controller

- LCM backlight LED:
  - Boost Controller for Serial mode LED (4~6)
    - Use external NMOS to boost the voltage to higher level.

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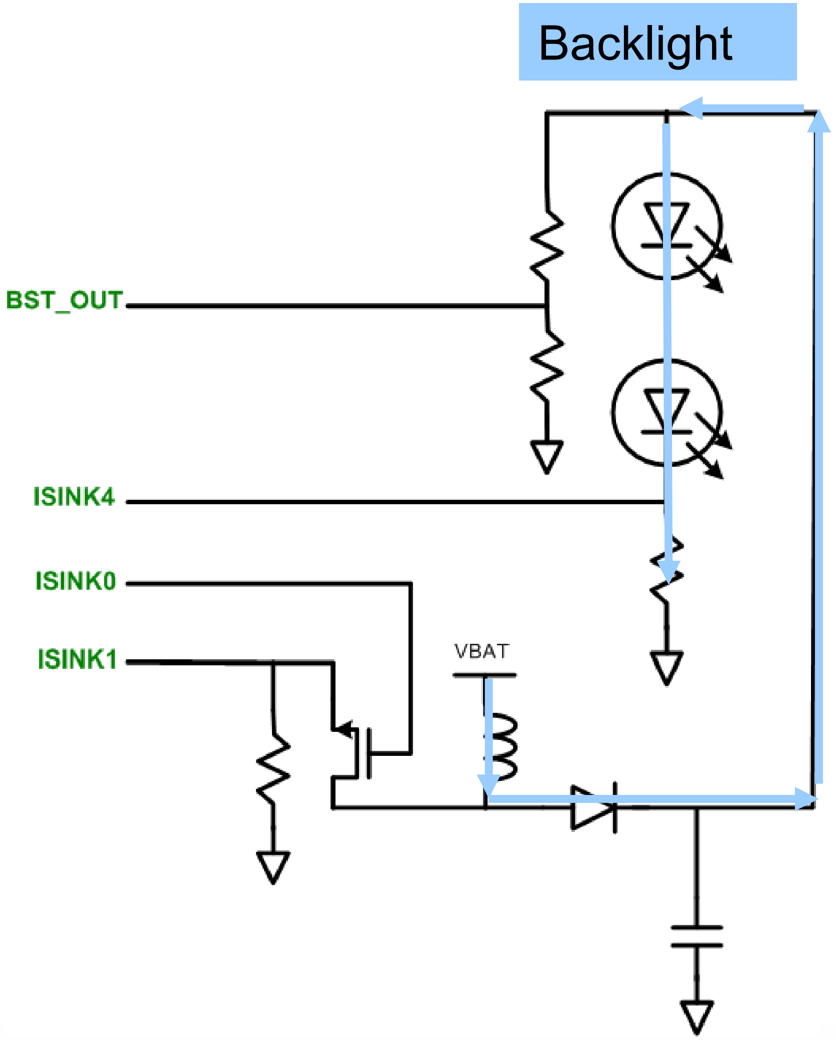
Function Description - Boost Controller



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Function Description – Current sink for backlight

- Current sink for LCM backlight LED:
  - Max. 5 current sink (For 3LEDs panel, please select this type)
  - No external component required
  - Current balance between channels
  - Individual channel current/enable control
- Note 1 : Luminance become lower when low battery.
  - Please follow “Criteria: Vth = Vf + 0.25V” to avoid this issue
  - Ex.
    - Set VBAT low voltage shutdown at 3.5V
    - Select LED (Vf < 3.5 – 0.25 = 3.25V) will keep luminance equal under normal operation range.
- Note 2 : PWM should set higher to prevent LCM panel flash. Suggest to set PWM frequency > 20kHz to prevent audible noise

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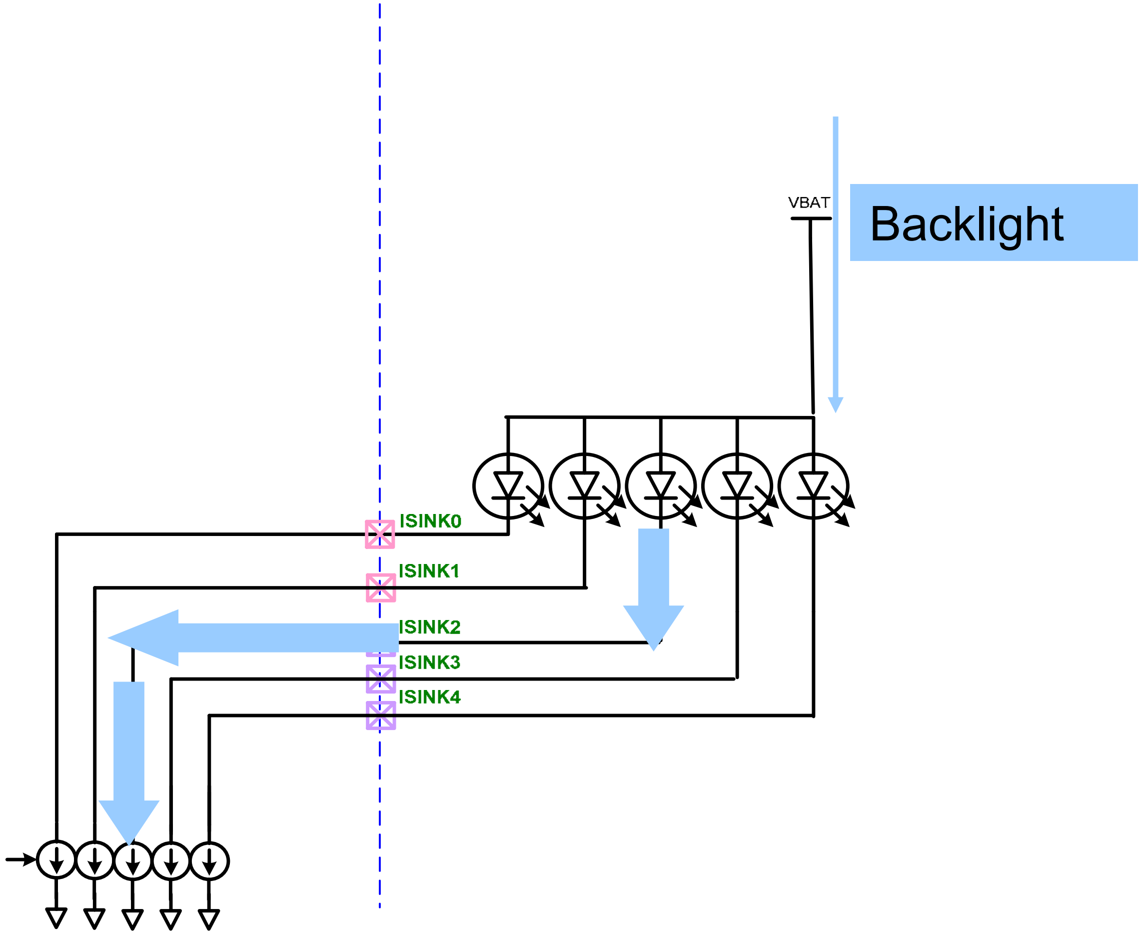
Function Description – Current sink for backlight



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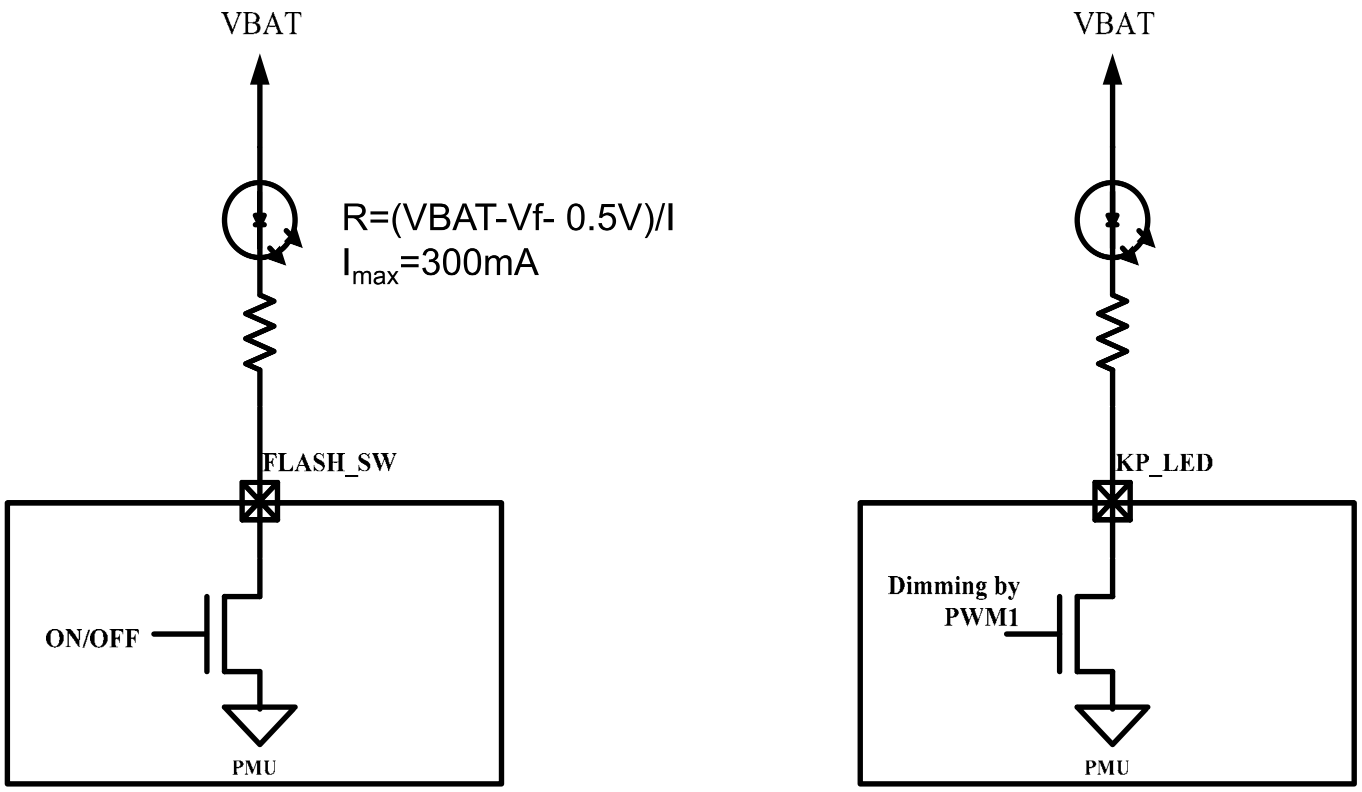
Function Description - Flash Light & Other Drivers



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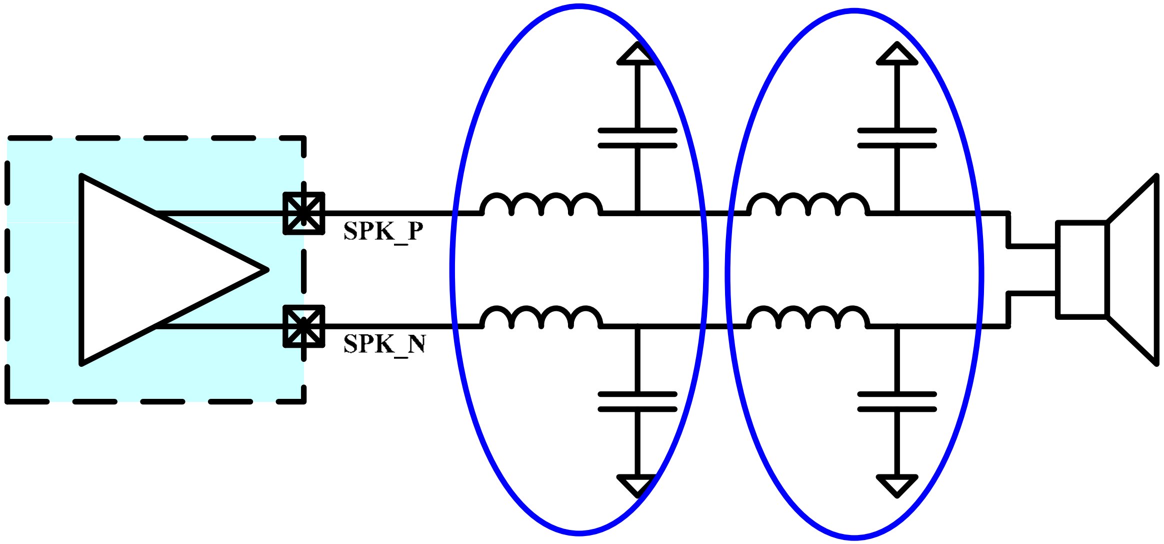
Function Description - Audio Amplifier Output Filter



- 2 filters are necessary.
- 1st filter need to be as close to chip pin out as possible.
- 1st filter need to locate inside shielding case.
- 2nd filter need to be as close to speaker.

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Content

- MT6236 Introduction
- Comparison
- Function Description
- **Reference design**
  - **Schematic**
- Appendix

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Typical Application

MT6236 Features		Vout	I_max	Application
LDO	VCAM_A	1.8/2.5/2.8	250	Camera module, AF module
	VCAM_D	SW Setting	100	
	VMC	2.8/3.3	100	Memory Card
	VSIM2	1.8/3.0	100	SIM2
	VIBR	SW Setting	200	Vibrator
Driver	Boost controller	SW Setting (max. 21V/20mA)		4~6 series LEDs for BL
	Current sink	100mA		Max. 5 parallel LEDs for BL
	KP_LED	150mA		KEYPAD
Audio Amplifier	Class D	0.9W at 4.2V		Single Channel

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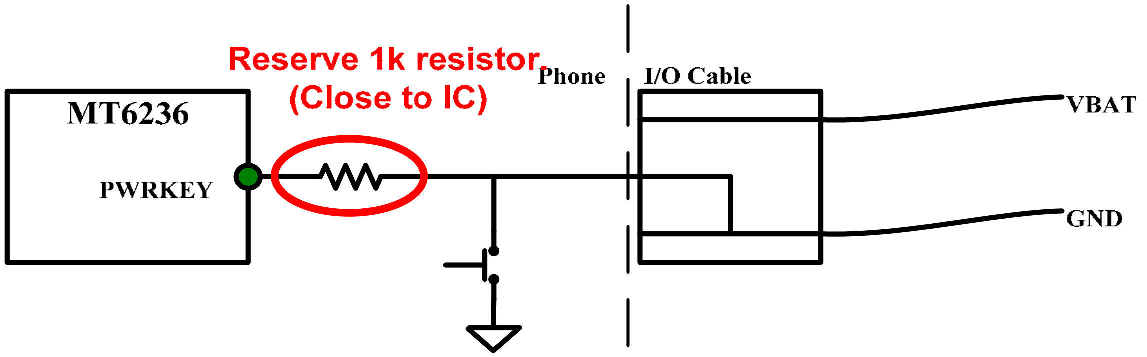
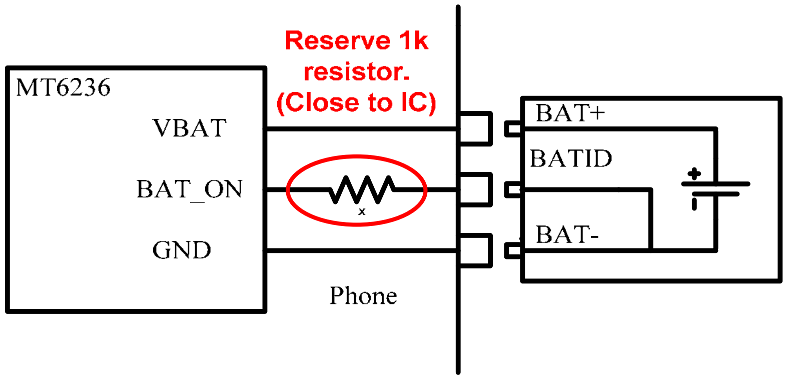
Reference design - Schematic
IC Protection: PWRKEY and BAT_ON



Please reserve 1k resistor on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

Please reserve 1k resistor on phone PCB to protect **BAT_ON** pin if BAT_ON is used to detect battery.



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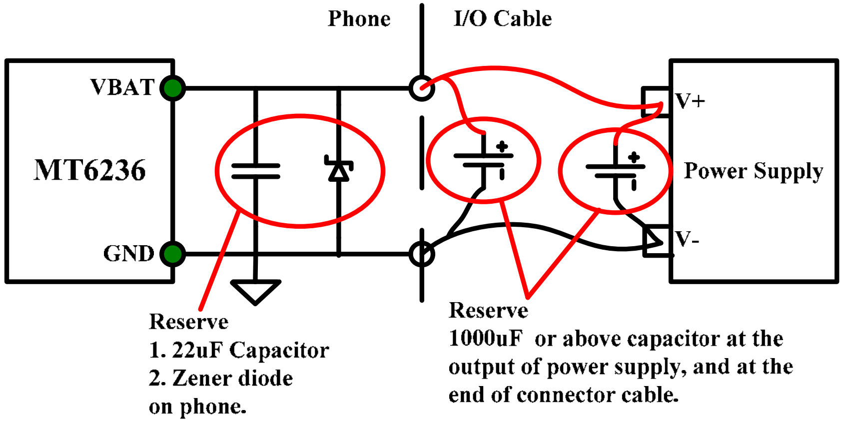
Reference design - Schematic IC Protection: VBAT



MT6236 has lower VBAT voltage rating. (Max. 4.3V.) Some protection should reserve to prevent the damage by voltage surge.

•Design notice in Phone side:

1. At least 22uF capacitor.
2. Add Zener diode (5.1V/500mW) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6236.

Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.

Notice: Using 5.1V zener will introduce some leakage when VBAT = 4.2V.

•Design notice in Power Supply side:

Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible. Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

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Zener Diode Selection Guideline

Selection Guideline

- 500mW zener diode has lower ZZT than 200mW and can sink more exceptional surge voltage/current.
- MT6236 must selcet 5.1V/500mW zener to enhance VBAT pin protection.
- Ir<100uA @Vr=4.2V, Ta=25 ° C, Using 5.1V zener will introduce some leakage when VBAT = 4.2V. Large Ir current will introduce more leakage current.

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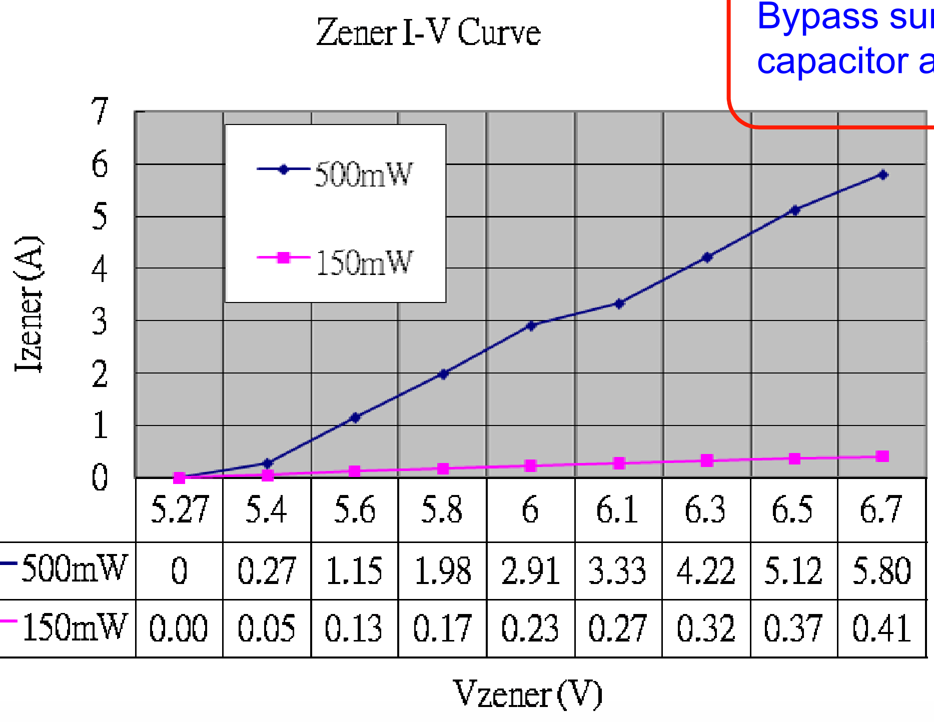
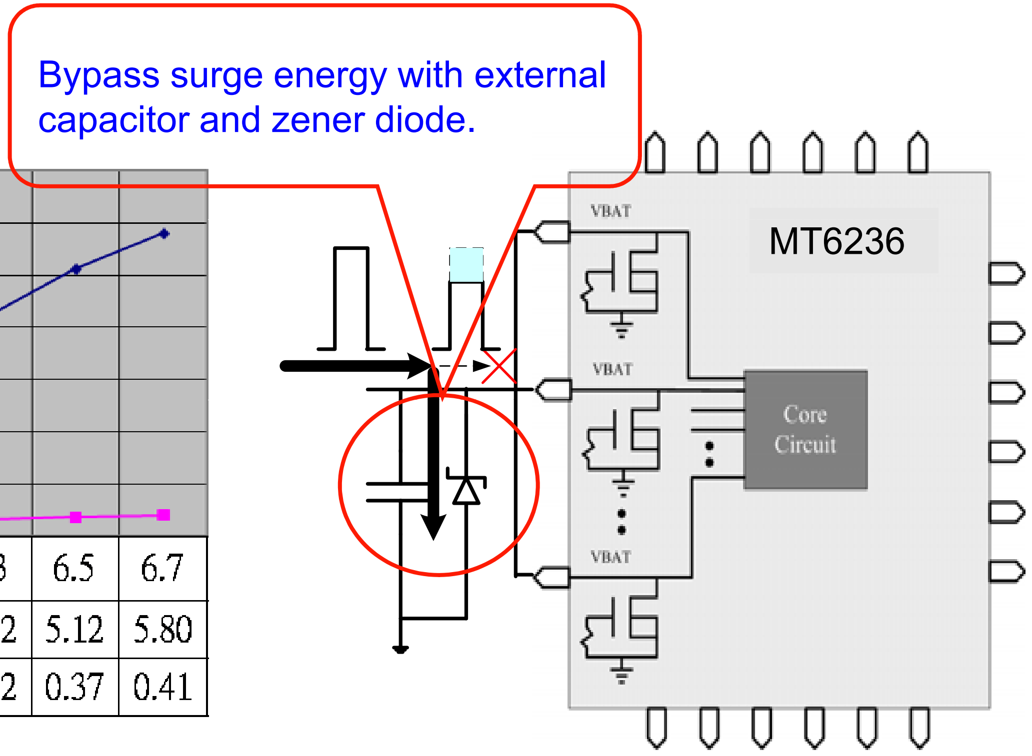
500mW Zener diode

- Change Zener diode to 5.1V/500mW
  - 150mW zener has similar current sink capability, can only release part of the external pulse energy.
  - 500mW zener can share more than 90% of external energy.



	5.27	5.4	5.6	5.8	6	6.1	6.3	6.5	6.7
500mW	0	0.27	1.15	1.98	2.91	3.33	4.22	5.12	5.80
150mW	0.00	0.05	0.13	0.17	0.23	0.27	0.32	0.37	0.41



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Zener Diode Validation List

- For design in,please notice the parts shipping delivery time.
- The latest validation list, please access the MTK BBS web.

Item	Vendor	Part number	Power (Watts)	Package	IR(uA) @VR=4.2V	Contact Window
1	On semi	MMSZ5231BT1G	500mW	SOD123	9	Tony Kao, 886-2-23761153 886-987-265-997 Email: tony.kao@onsemi.com
2	JIANGSU CHANGJIANG (长电科技)	MMSZ5231B	500mW	SOD123	72	Mr. Chan 0510-86858061 13601525970 E-mail: cyz@cj-elec.com
3	Prisemi	PZ3D4V2H	500mW	SOD323	11.5	欧新华 Mobile:18602108386 Tel: +86-21-60870158-8018 Email: ken.ou@prisemi.com
4	Prisemi	PZ5D4V2H	500mW	SOD523	4.85	
5	Vishay	MMSZ4689-V	500mW	SOD123	7	Mike_Wang 886-911313660 mike.wang@Vishay.com
6	Crownpo	CDZ55C5V1SM	500mW	0805	10.2	陳富榮Sam 138-12888205 Email: sam@sh-selmag.com

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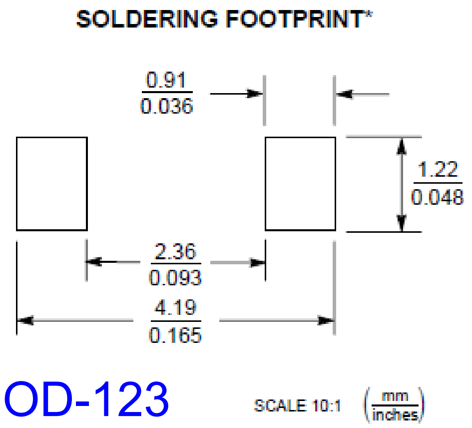
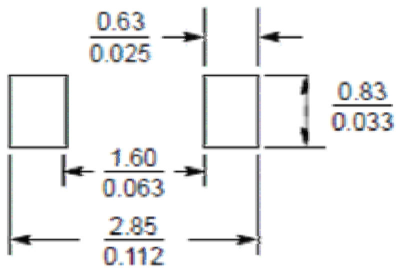
Co-Layout

- For 2nd source parts concern, co-layout is flexible to select parts vender.
- SOD-123 and SOD-323 are most popular package of 500mW Zener and can co-layout . For thermal dissipation concern, SOD-123 and SOD-323 are fist choice and then SOD-523.
- For safety operation area, please notice the steady state power rerating and should exposed pad to a large copper.



SOD-123



SOD-323

SOD-123/ SOD-323

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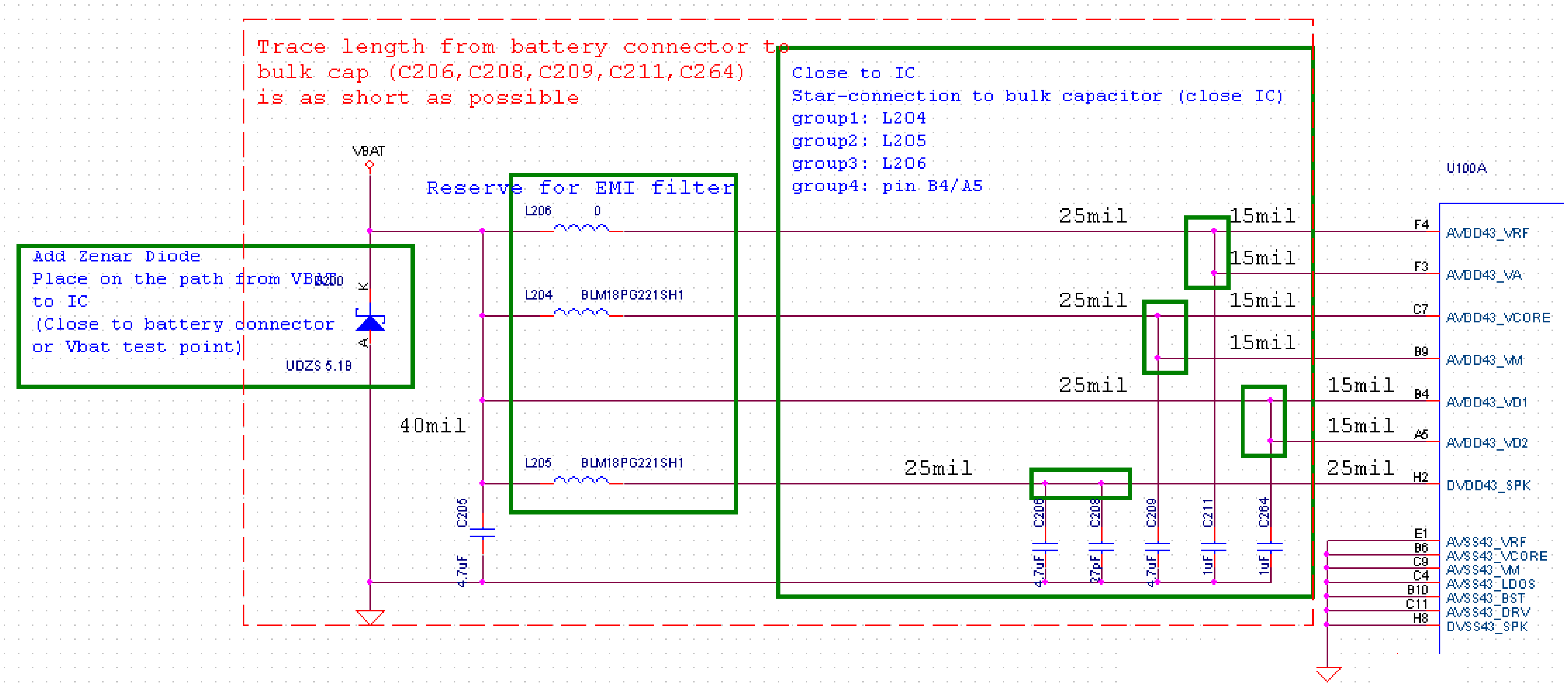
Reference design - Schematic VBAT Input Filter



- VBAT input should reserve enough filter to prevent interference to RF performance.
- All bypass cap. should be as close to MT6236 IC as possible
- Bead selection: Rated Current > 1000mA, DCR < 0.10ohm

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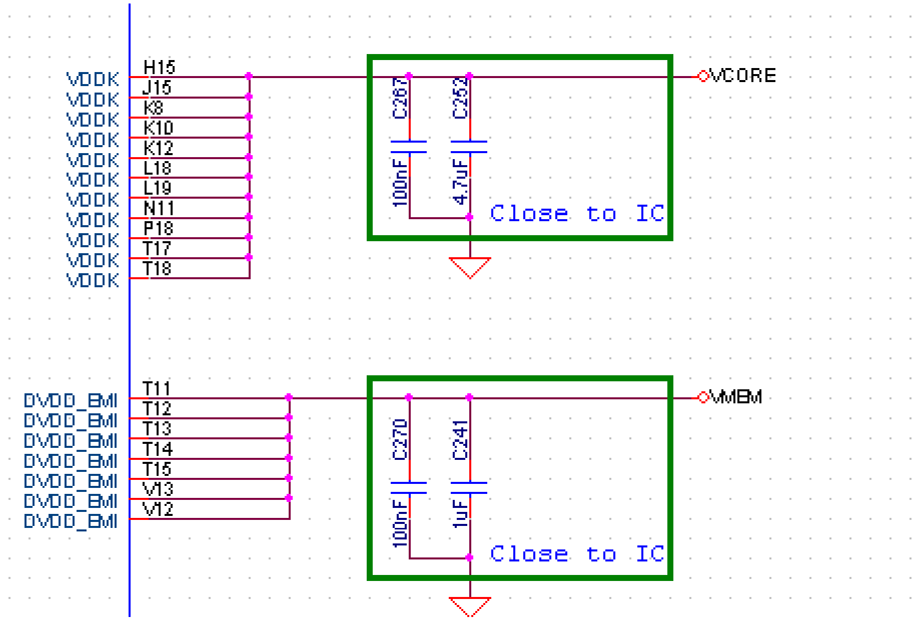
Reference design - Schematic
Bypass Capacitor: Vcore and VM



- Reserve enough bypass capacitors both at Vcore and VM to obtain good system stability.

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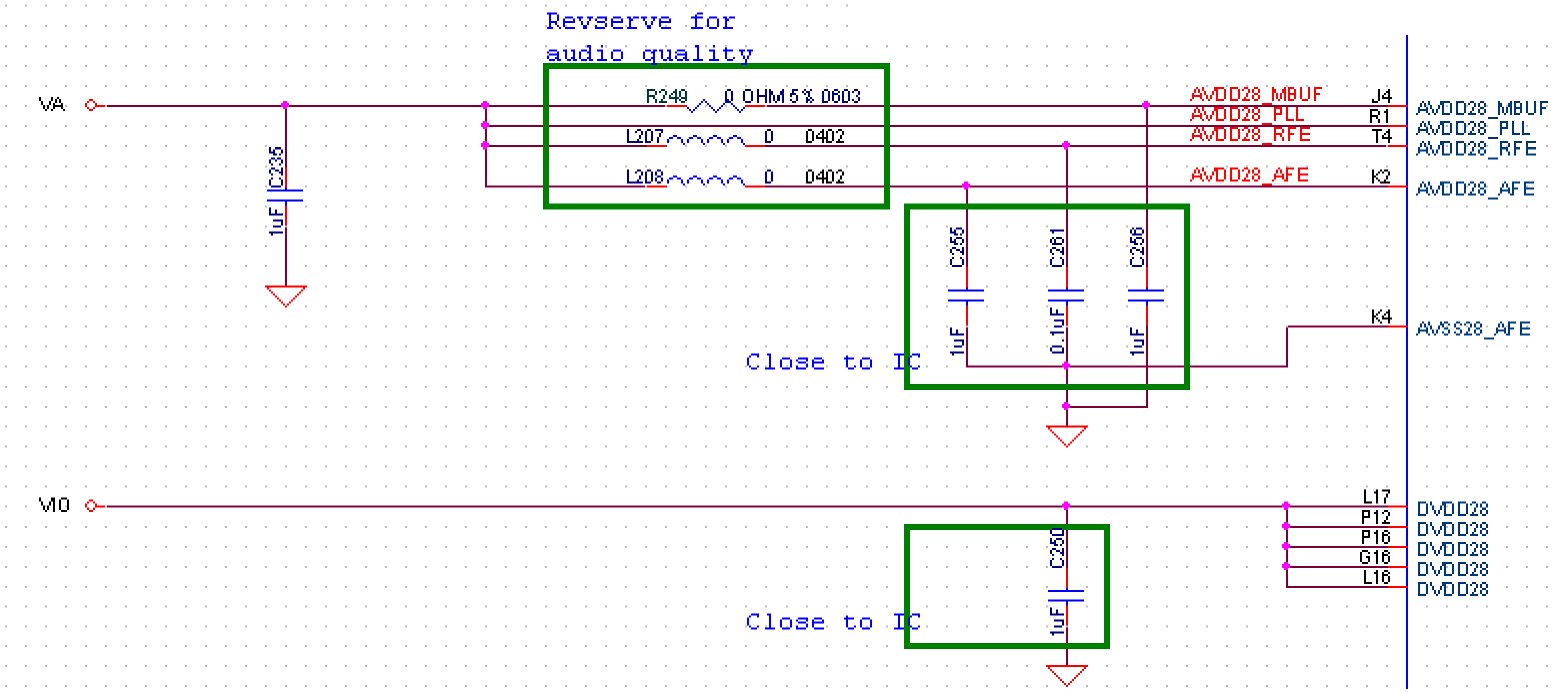
Reference design - Schematic
Bypass Capacitor for AVDD and VDD



- Reserve 0 ohm resistor for audio quality.
- Reserve 1uF for I/O power input.

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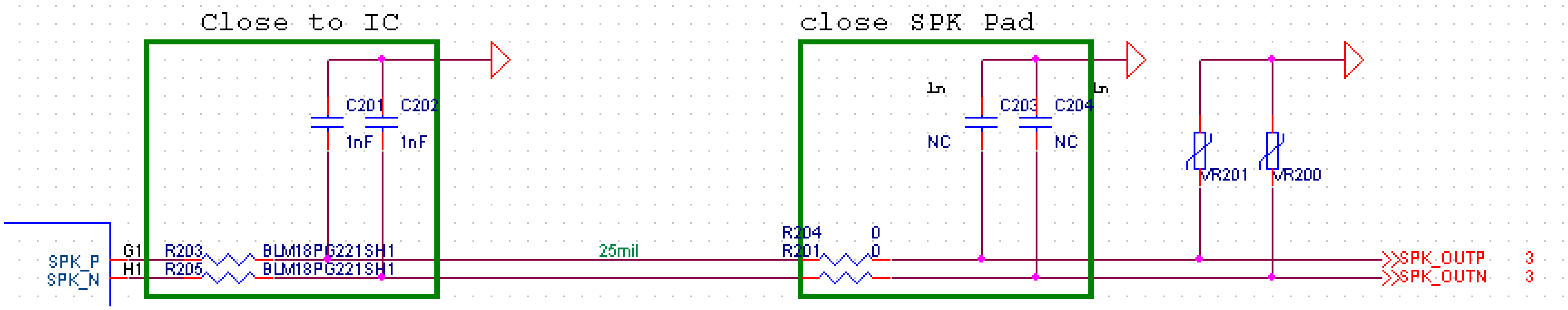
Reference design - Schematic
Class-D Audio Amplifier Output Filter



- Reserve 2 stage filter at output stage of Class-D to prevent interference to RF performance.
- 1st stage filter should be close to IC
- 2nd stage filter should be close to loud speaker.
- All the traces from IC to 2nd stage filter should not exposed to prevent interference to RF performance.
- Bead selection: Rated Current > 1200mA, DCR < 0.10ohm

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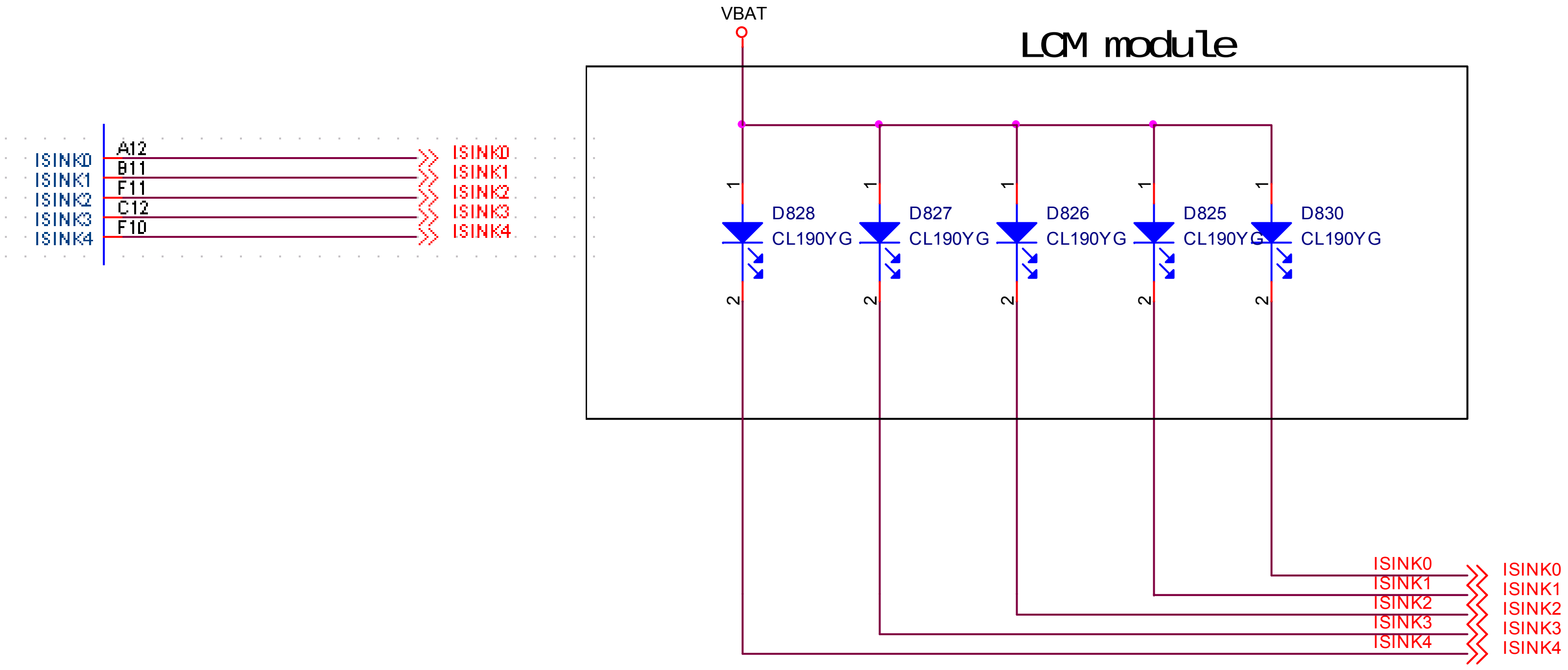
Reference design - Schematic

Current Sink for Parallel Backlight LCM



- Width and length of trace of ISINK0~4 should be consist between IC and LCM
- voltage table

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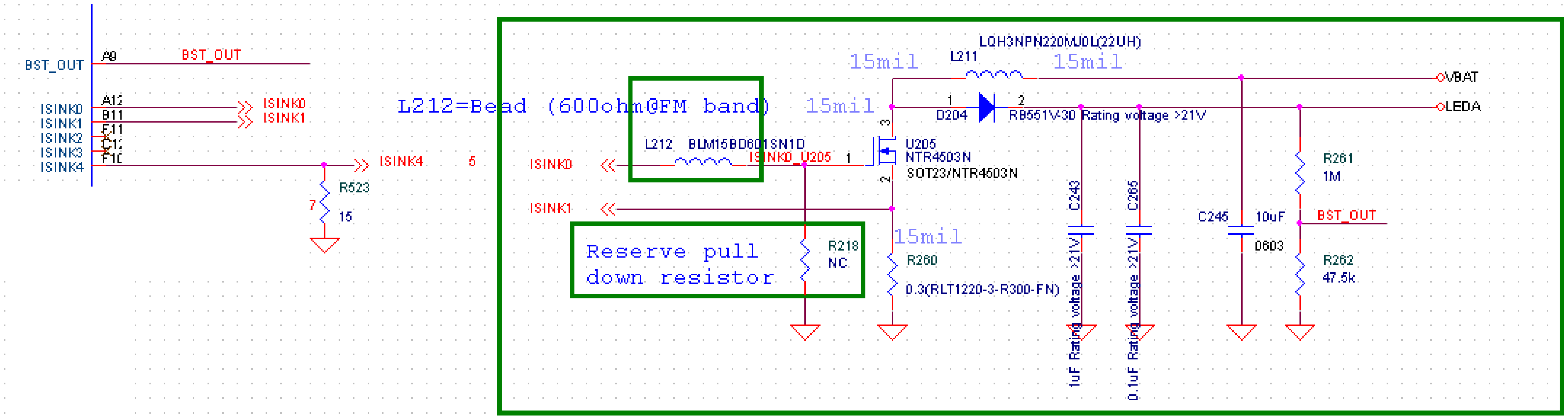
Reference design - Schematic
Boost Controller For Serial Backlight LCM



- Reserve L212 to prevent interference to FM performance.
- Bead selection: Impedance> 600 ohm@100MHz

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Design Notice - Pulse Charging

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Pulse Charging

- Feature
  - Maximum input voltage up to 30V
  - Support low cost linear and Nokia adaptor charger(9.3V)
  - Meet 2010 China charger standard(12V OVP)
  - CC mode current control
  - Constant current pre-charging
  - Charger OVP and battery OVP
  - Pre-charge/CC safety timer
  - Watchdog timer

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MT6236 Charging Feature Comparison

Feature \ Chip	MT6253	MT6235	MT6236
Charging type	CC-CV	CC-CV	Pulse Charging
Maximum charger input voltage	9V	9V	30V
Support battery type	Li-ion	Li-ion	Li-ion
VCHG OVP	7V	7V	10.5V (Default off)
CV	4.2V	4.2V	4.2V comparator
CC	160mV/R	160mV/R	160mV/R
Pre_ charge	24mV/R	20mV/R	20mV/R
Battery OVP	4.3V	4.3V	4.35V
Watchdog timer	Yes	Yes	Yes
Pre-charge safety timer	NO	NO	50 minutes
Passed element	P-MOSFET +SD	P-MOSFET +SD	BJT+ N-MOSFET
Pre-charge/CC overlap	Yes	No	Yes

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Design Notice – Charge Current Setting

		MT6318	MT6223	MT6235		MT6236
Sense Resistor		0.2 Ohm	0.2 Ohm	0.2 Ohm	0.1 Ohm	0.2 Ohm
Pre-Charge		62.5	62.5	100	200	100
CC	0	62.5	62.5	62.5	125	100
	1	90	90	90	180	200
	2	150	150	150	300	400
	3	225	225	225	450	425
	4	300	300	300	600	550
	5	450	450	450	900	650
	6	650	650	X	X	700
	7	800	800	X	X	800

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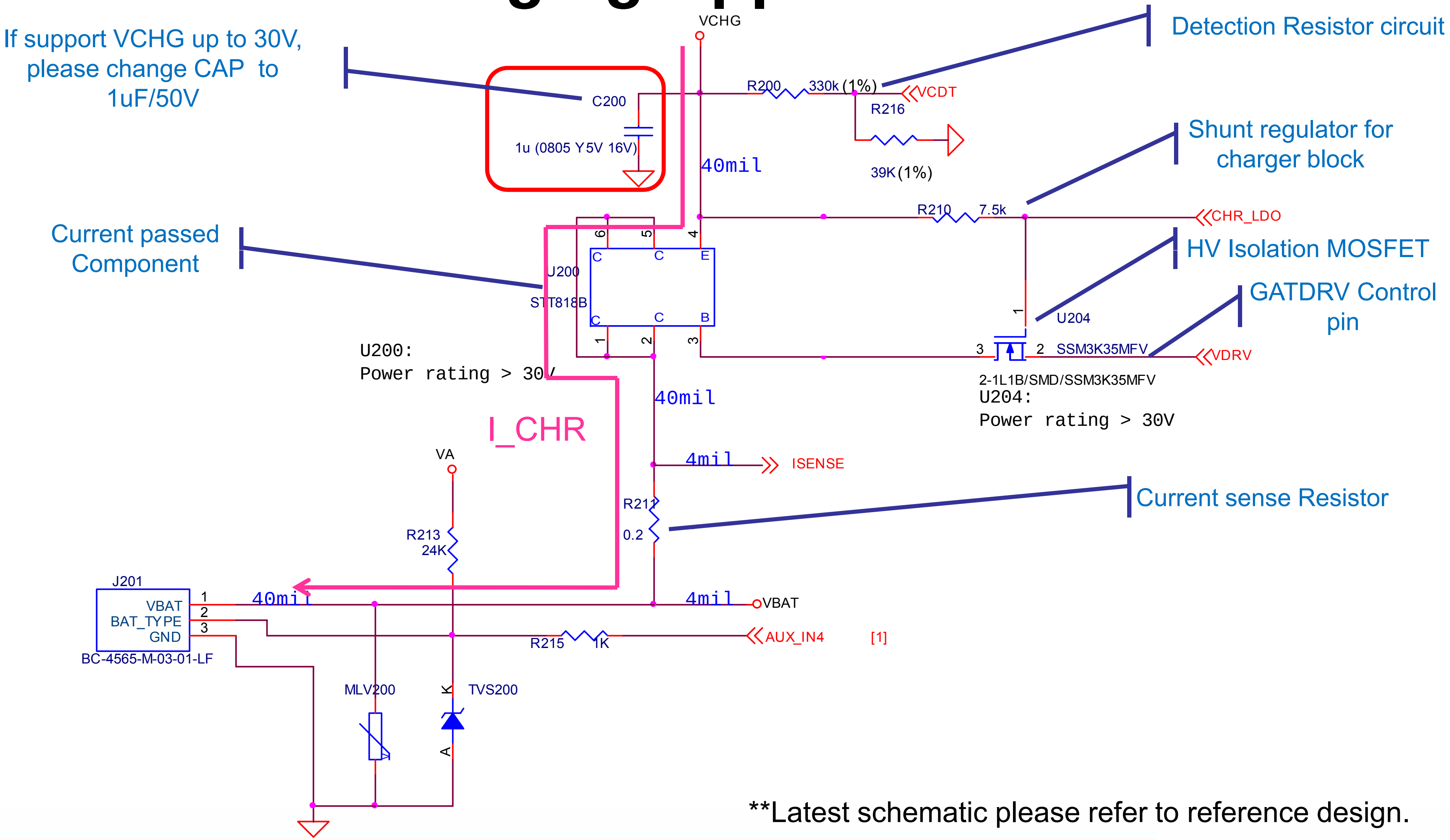
MT6236 Charging Application Circuit



**Latest schematic please refer to reference design.

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Pins Description

Pin	Function
VCDT	Charger detect, the V_CHG detection threshold voltage is 4.3V at charge off state
CHR_LDO	Charger power supply source and it’s a 2.8V shunt regulator
VDRV	Charge passed element control pin
BATSNS	Battery voltage sense pin
ISENSE	Current sense pin
BATON	Battery detection pin. If this pin is large than 2.5V will disable charging.

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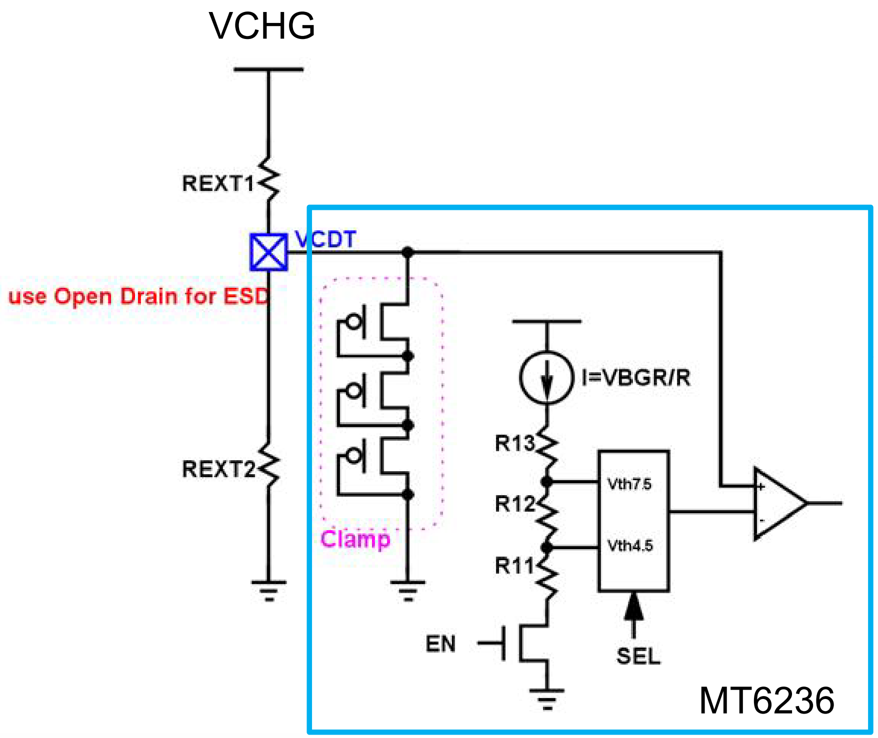
Charge Detection

- Charger detect, the detection threshold voltage is 4.3V at charge off state.
- Charger over voltage protection HW default is disable, SW can customize. (Default is 7.5V)



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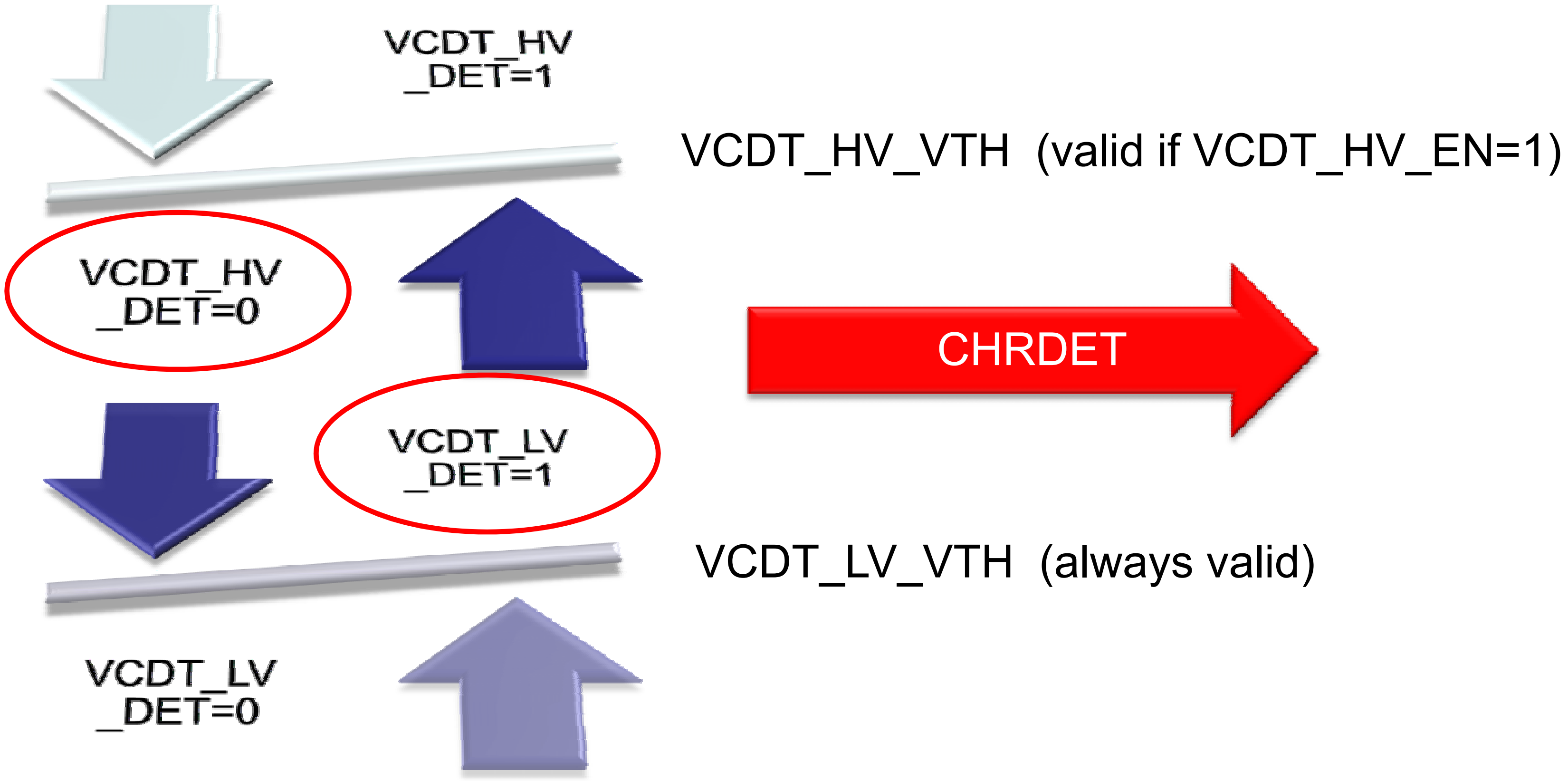
Charger Detection



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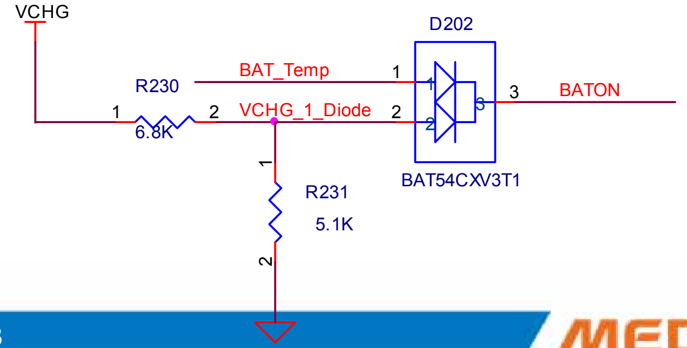
Charger OVP

- Charger over voltage protection HW default is disable.

  After power on, SW will configure “VCDT_HV_VTH”

	Min	Typical	Max
09	5.7	6	6.3
10	6.175	6.5	6.825
11	6.65	7	7.35
12	7.125	7.5	7.785
13	8.075	8.5	8.93
14	9.025	9.5	9.97
15	9.975	10.5	11.02

- Other, adding below circuitry to increase a OVP path .
  – BATON toggle threshold is 2.5V.



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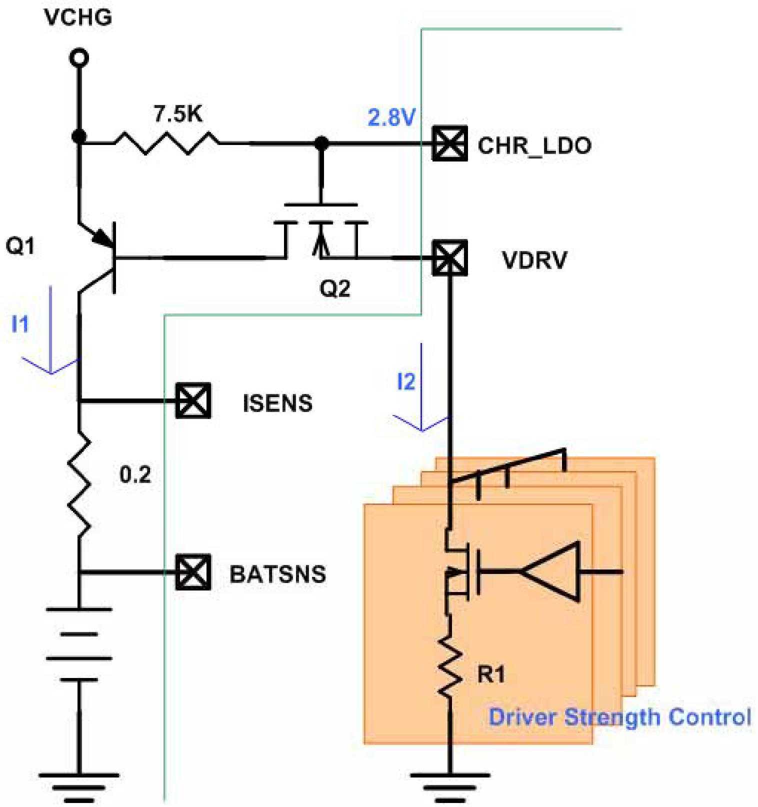
VDRV Driving Control

- If Q1 does not go into saturation, $I_1=\beta_1 x I_2$.
- Assume I_1=450mA, β_1=200

  => I_2=2.25mA
- If Q1 goes into saturation, look up the characteristic table to get the relationship between I_1 and I_2.
- Build in 256 steps CSDAC for current driving control.



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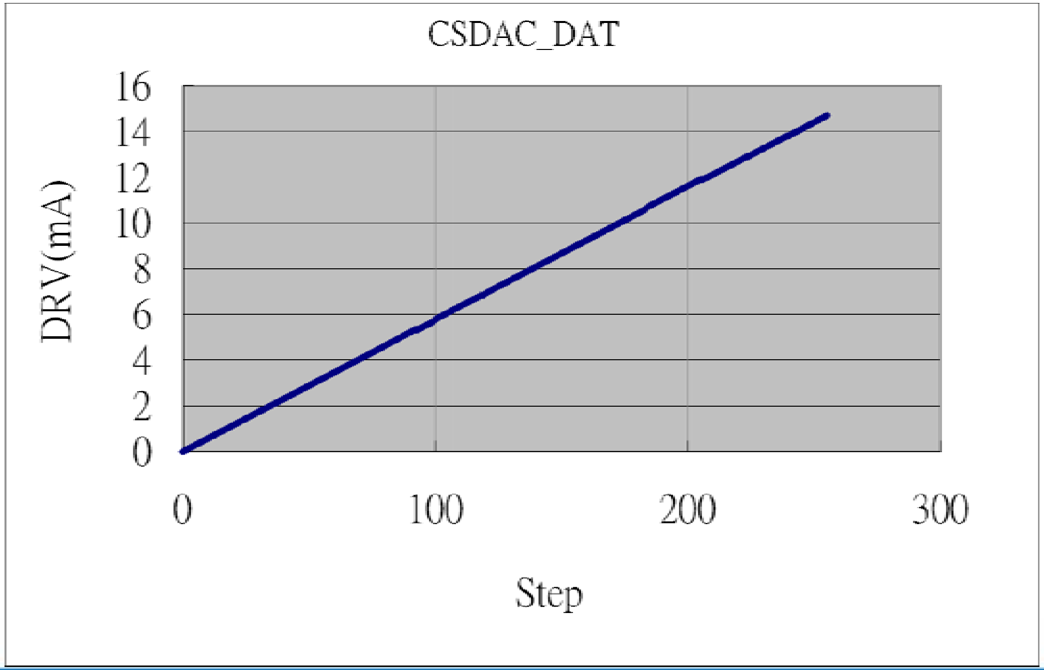
CSDEC

- Charge current =β_1*I_CSDEC
  - I_CSDEC (maximum)=14.8mA.
  - I_CSDEC selection
    - 1 LSB =55uA. Current step = 55uA*200(β_1)=11mA
- DC Current Gain(β) must be 100~300 at Ic=0.5A



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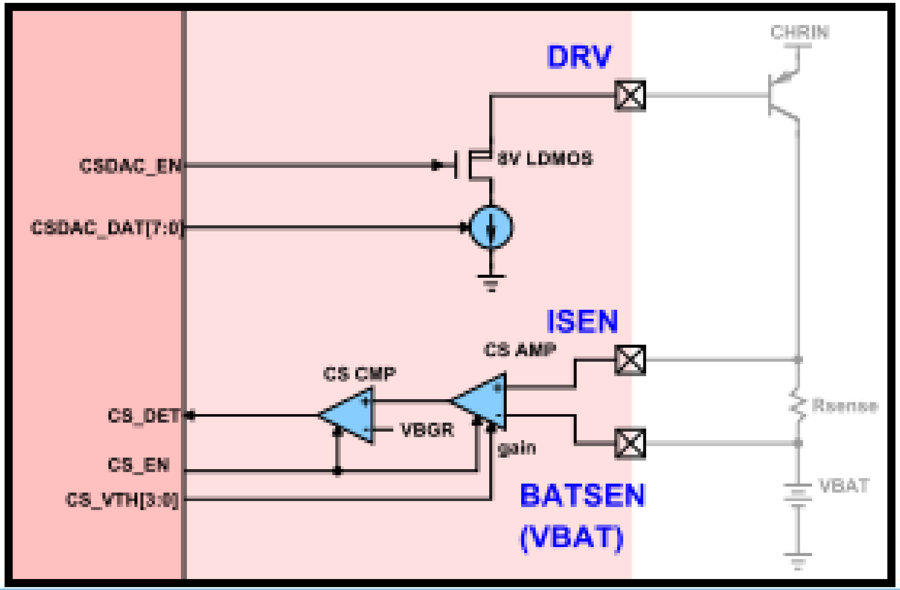
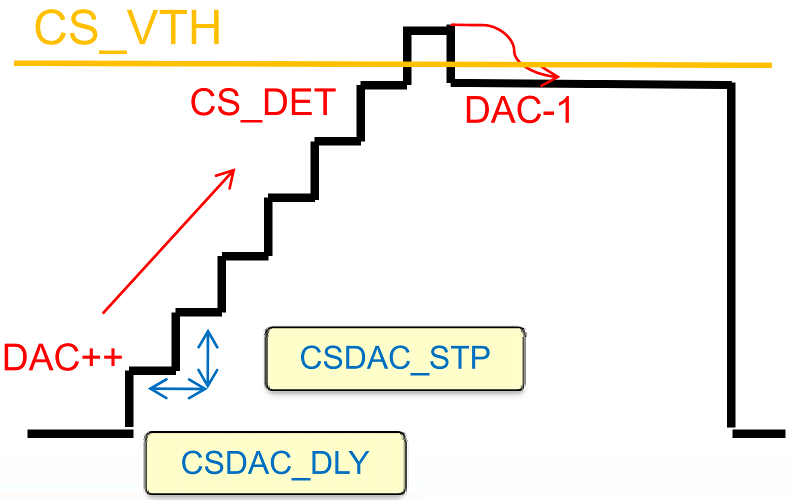
CSDEC Driving Control

- CSDEC Enable Control
  - CS_VTH =>PCHR_AUTO (Auto mode)
  - CS_VTH =>DAC_EN
- Programmable soft start
  - CSDAC_STP
  - CSDAC_DLY





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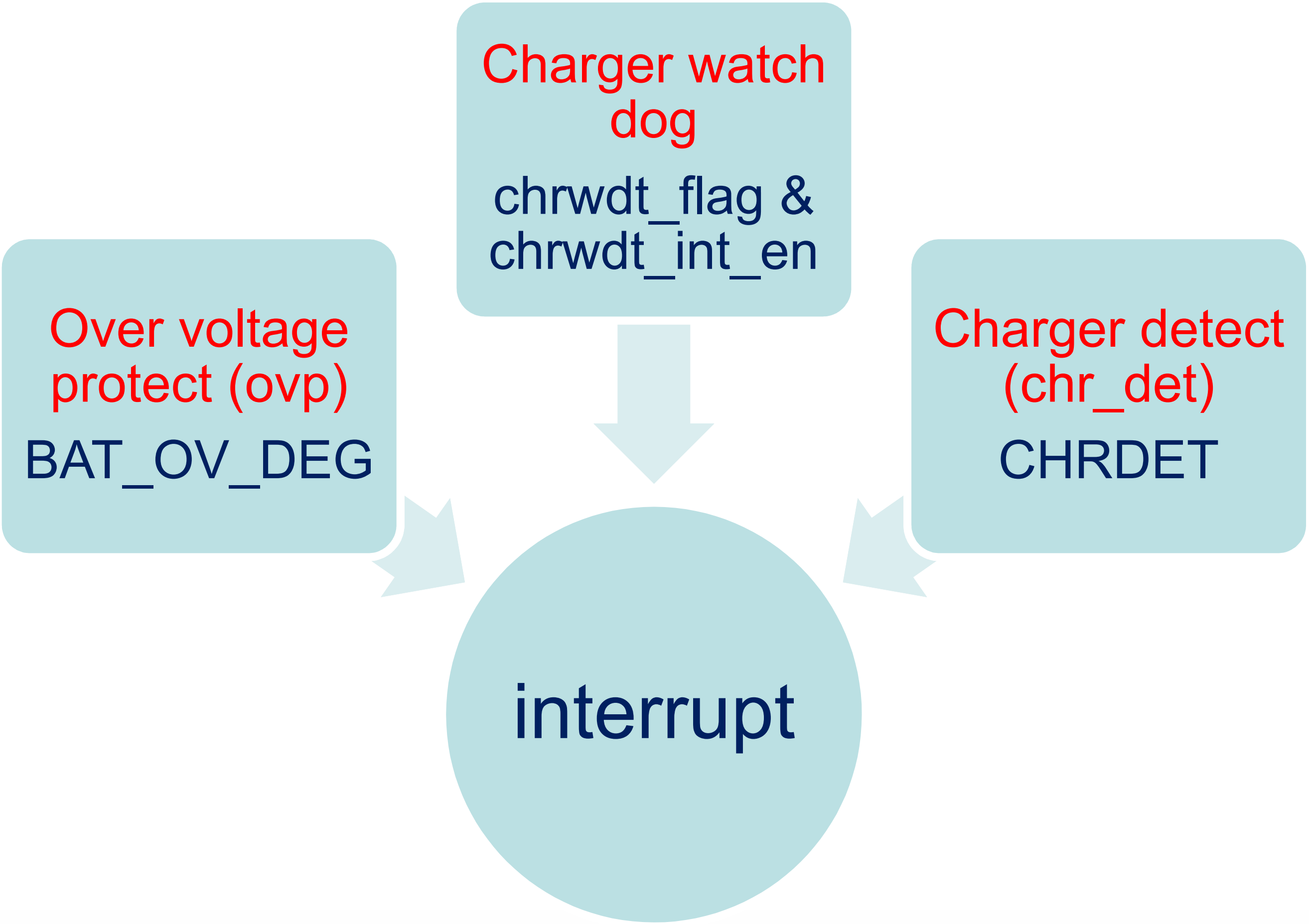
Interrupt



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MT6236 Pulse Charging State

- PreCC (H/W)
- PrecCC VBAT < 3.4V
- CC: VBAT > 3.4V
- CV: VBAT > 4.1V
- Post-Full: Change charging duty (Smaller duty)
  - Accumulate 6 times PMU CV status = 1 (VBAT >= **VBAT_CV_VTH**)
- Charging complete
  - >CV after waiting 90secs or 30mins time out
- Pause: talking state

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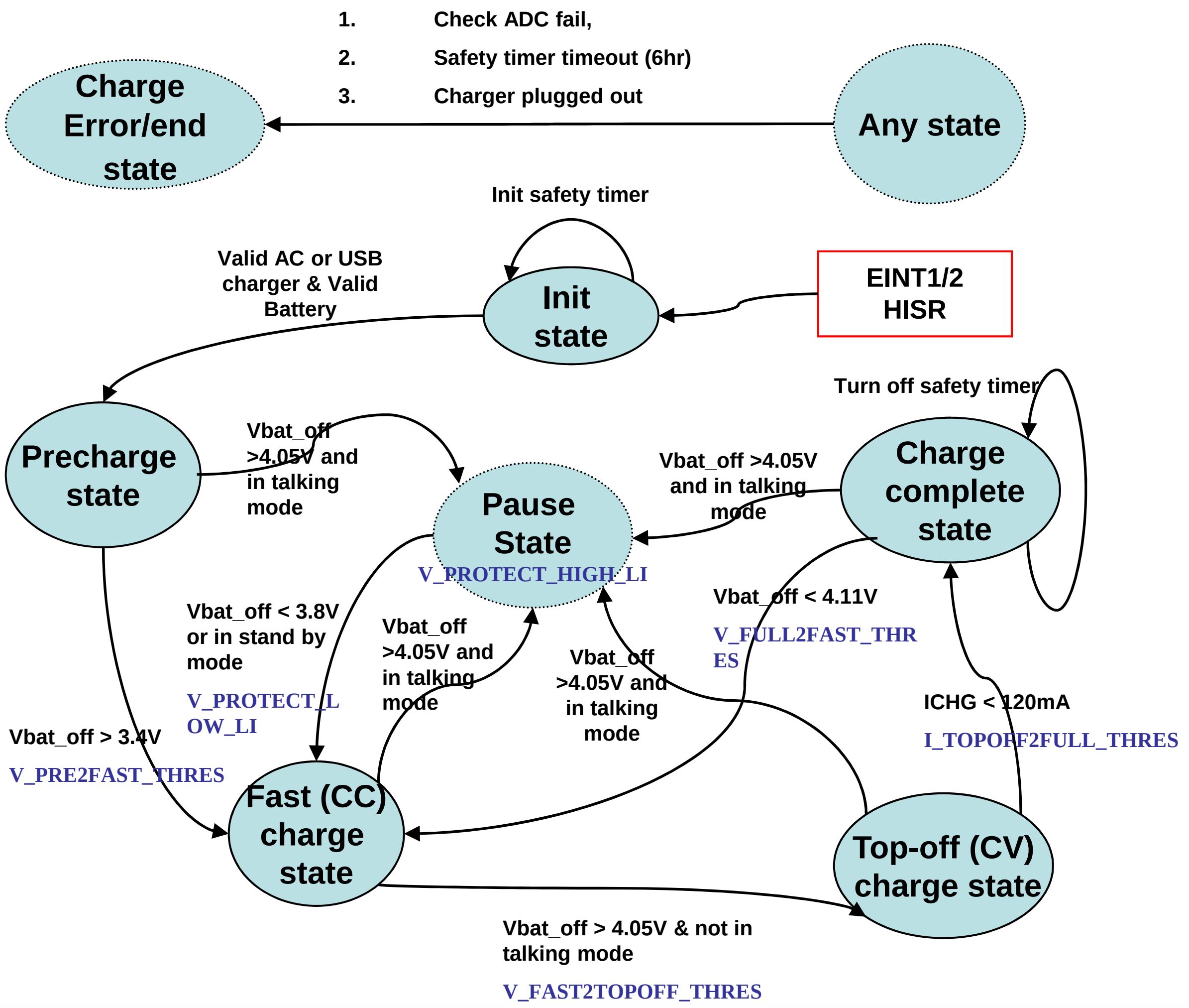
Original Charging State

- State diagram



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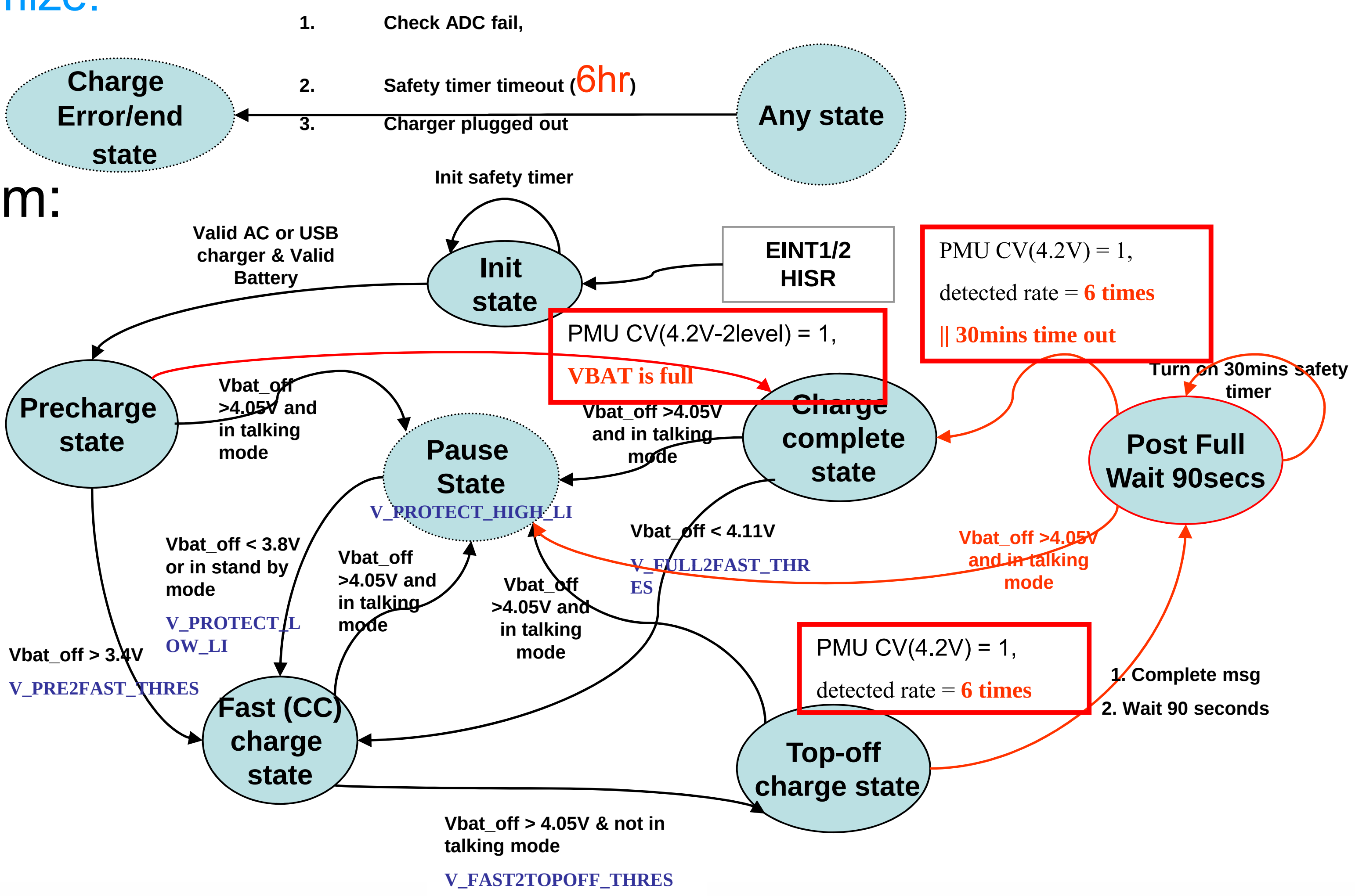
New Charging State

- Please refer to pulse charging SW customize programming guide to customize.

State diagram:



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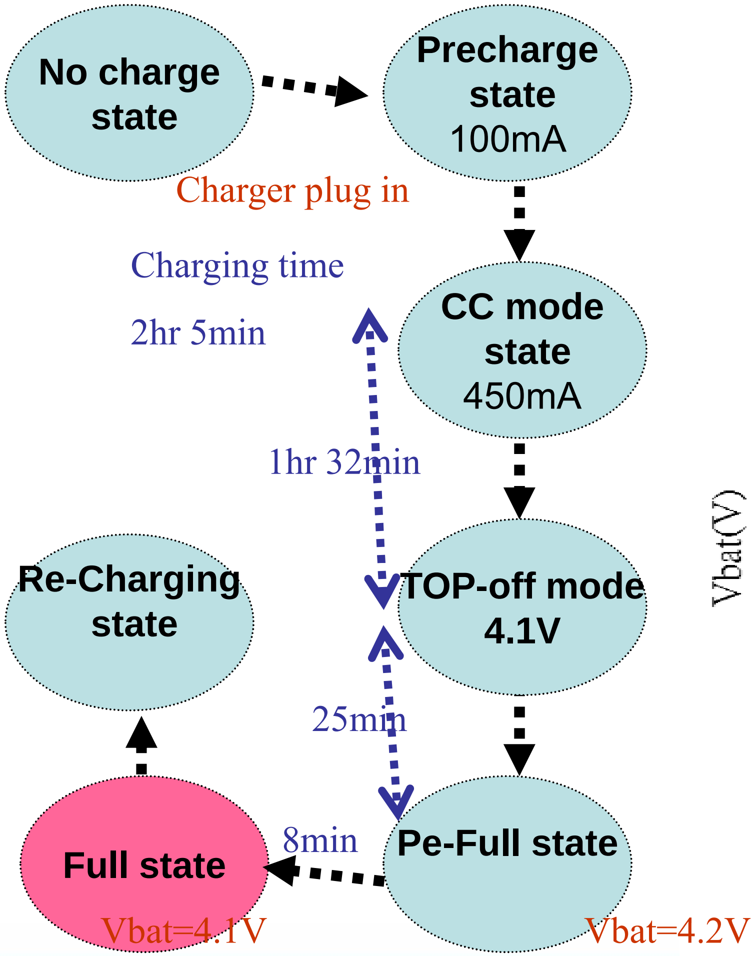
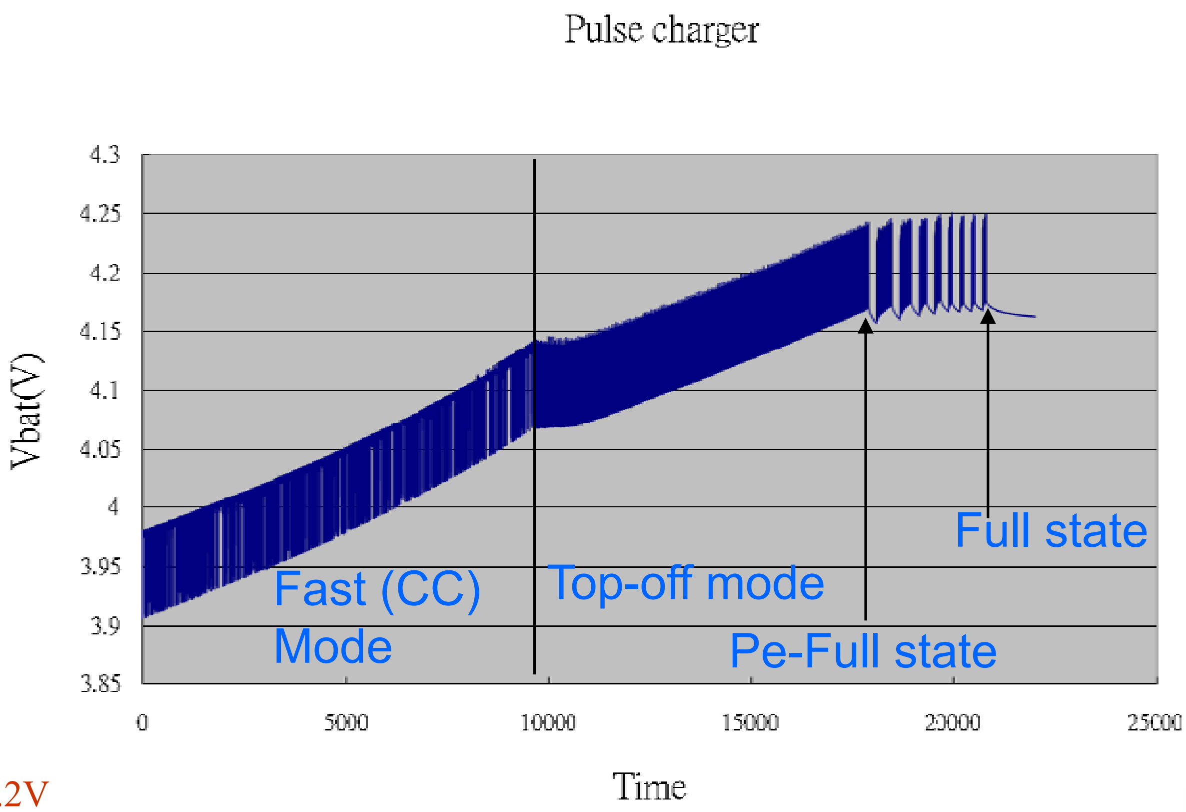
Pulse Charge Charging Curve





Application Limitation

- Must have "Off duty" to detect charger plug-out.
  - Otherwise has reverse current and can't detect charger plug-out
- BJT (DC Current Gain) will effect current step and accurate
  - Smaller "DC Current Gain" get more accurate.
  - Too small "DC Current Gain" to charge up zero voltage battery.
    - Vbat <1V, CSDEC will limit at 4 step(0.23mA).

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Component Selection Glide

- U200:Current passed Component
  - hFE (DC Current Gain) is 100~300 (Typical 200 @-20~80 ^{0}C) at Ic=0.5A
  - For thermal dissipation concern, the U200 power dissipation must be large than 1W.
  - VCE(Collector-Emitter Voltage) ≥30V
  - Ic >0.8A (Depend on application)
- U204 N-MOS
  - Vgs threshold <1.5V @Id=0.1mA
  - VDS>30V (Depend on application)
  - RDS (ON) <10 ohm @ID = 10 mA, VGS = 2.5 V
- C200 (VCHG input cap)
  - If want to support VCHG up to 30V, please change CAP to 1uF/50V.

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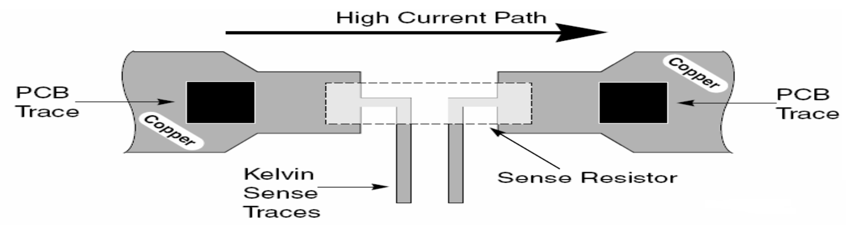
Charger Layout Notice:

- C216 CHR_LDO decouple cap close to IC.
- R211 (Current sense resistor)close battery connector and trace is 40mil(star connect to connector)
- The exposed pad of the U200(Current passed component) should connect to a large copper ground plane to get good thermal performance.
- ISENSE and BATSNS should be connected as the below figure.
- The trace from Rsense to battery connector should not share with other VBAT traces.
- ISENSE/BATSNS should be routed as differential traces which are away from noisy signals.



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Design Notice - Bluetooth

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MT6236 BT Reference Design Circuit

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0 ohm Pad --> Reserve for BT/WiFi single antenna design

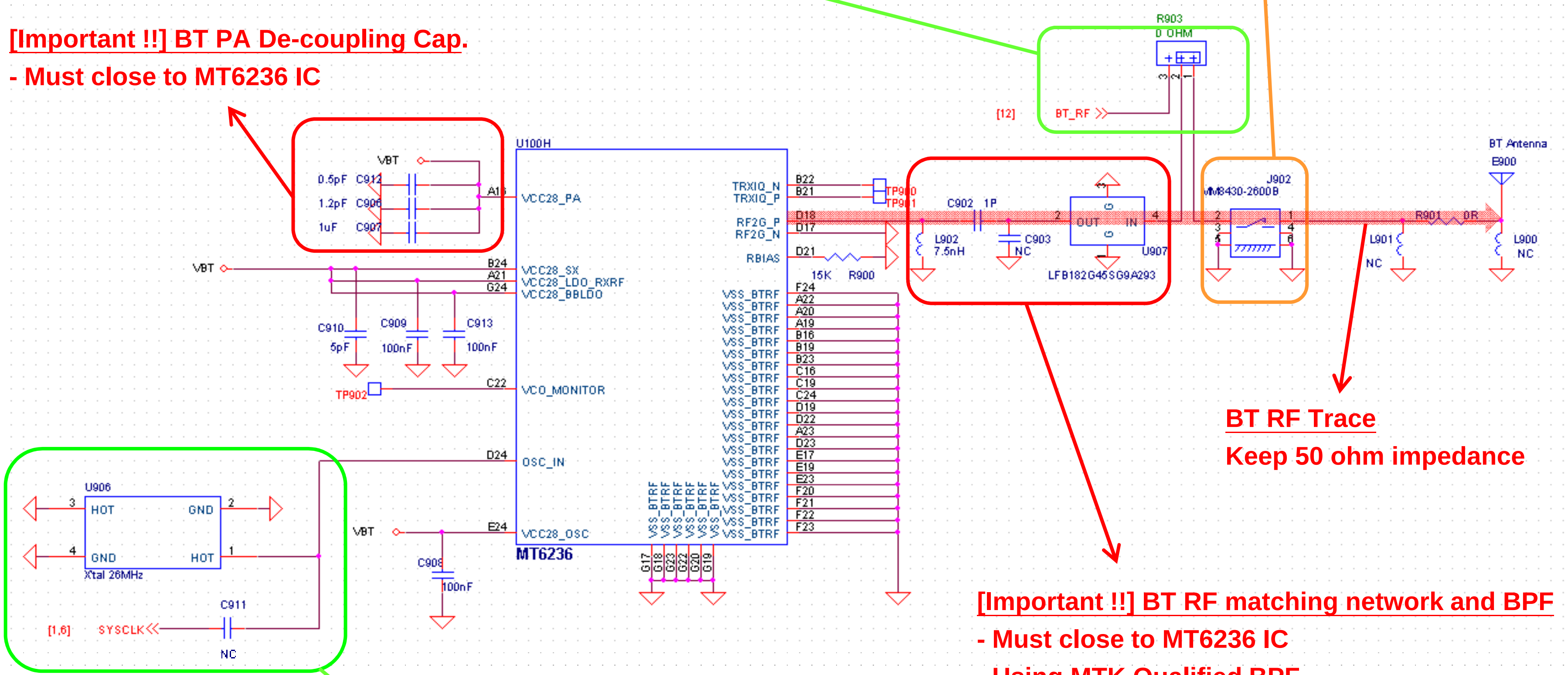
- BT/WiFi Dual antenna : R903=1-2
- BT/WiFi Single antenna : R903=2-3

RF connector :

For BT conductive performance testing

[Important !!] BT PA De-coupling Cap.

- Must close to MT6236 IC



BT RF Trace

Keep 50 ohm impedance

[Important !!] BT RF matching network and BPF

- Must close to MT6236 IC
- Using MTK Qualified BPF

26MHz reference clock source

- U906 --> Dedicated 26MHz X'tal for BT usage.
- C911 --> sharing 26MHz clock with OG/OE.

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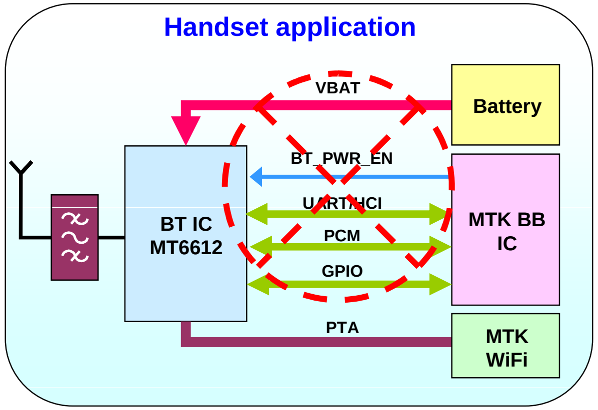
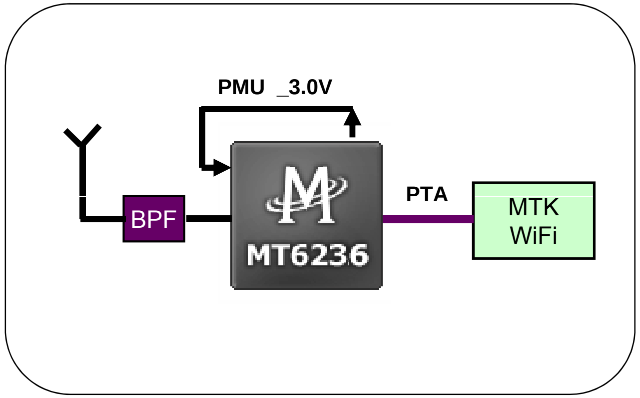
MT6236 BT Interface Design (1/2)

- Since the MT6236 features a highly integrated Bluetooth transceiver, **no need external interface to connect with Host .**

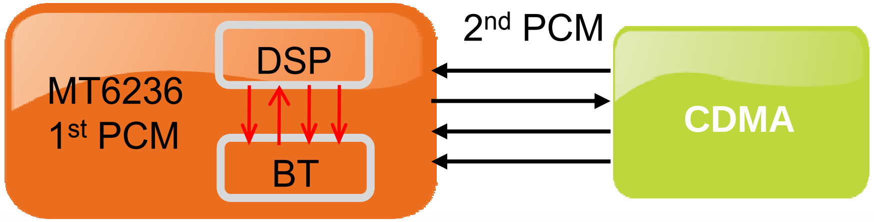
MT6612/MT6616



MT6236



- MT6236 support Dual-PCM interface.
  - In typical application, the audio interface between BT and DSP subsystem is connected with together in MT6236. **No external interface is required.**
  - For Dual mode handset, **2nd PCM is required. Finding the detail notices in the next page.**



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MT6236 BT Interface Design (2/2)

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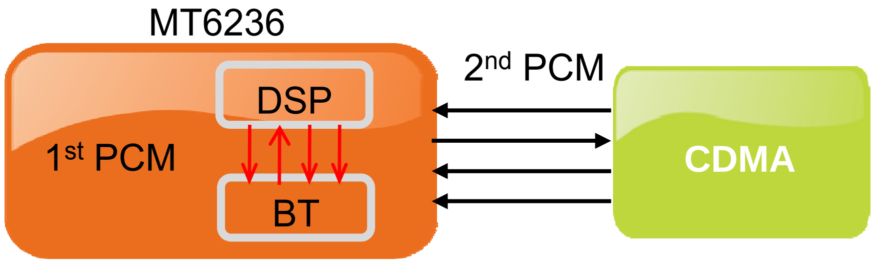
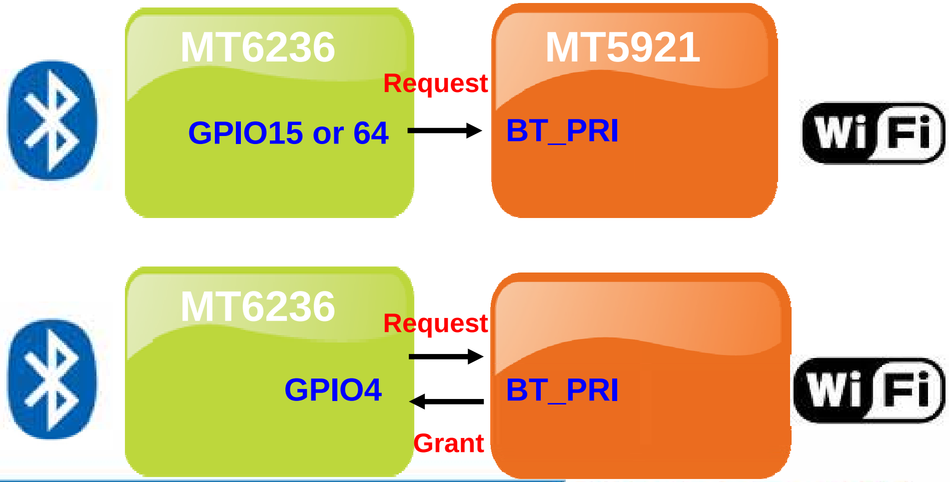
- Dual-PCM for G+C Application
  - PCM format (CLK=128K, Short/Long sync, MSB/LSB, etc) setting should be the same for G and C modem.
  - GPIO configure should also be careful to prevent unwanted leakage.

MT6236 Pin Number		
PCM	1st PCM	2nd PCM (Model)
PCM CLK	Internal PCM	N19
PCM OUT		M22
PCM IN		M23
PCM SYNC		L23



- MT6236 PTA interface.
  - MT6236 supports **Two-wire** and **Proprietary One-wire** protocol with proper configurations.

Signal	GPIO	Direction	MTK 1-Wire		Standard 2- Wire	
BT2WIFI_0	GPIO 15	Output	V		V	
WIFI2BT	GPIO 63	Input			V	V
BT2WIFI_0	GPIO 64	Output		V		V



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MT6236 BT Layout Guideline (1/2)

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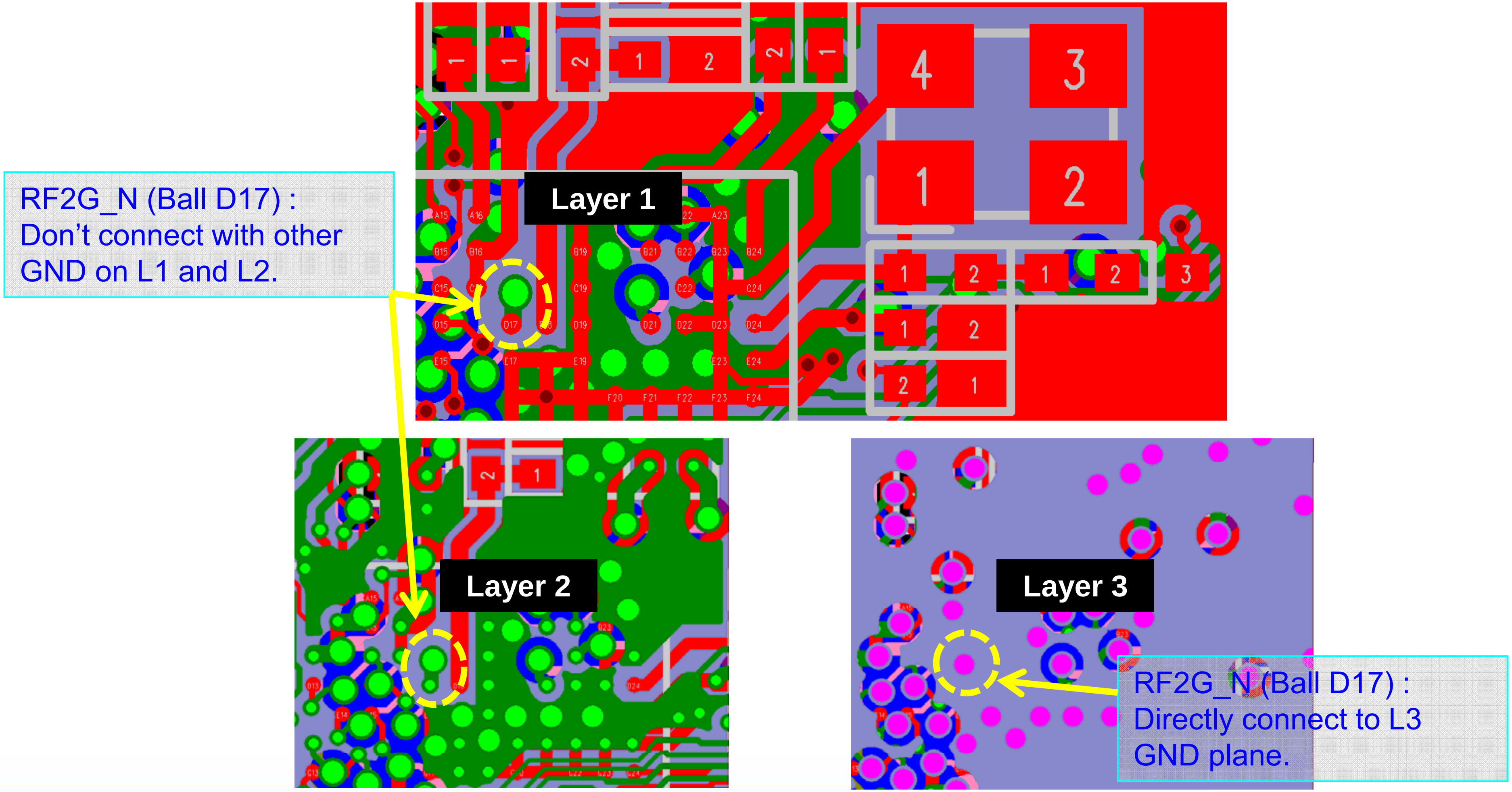
- The RF2G_N (ball D17) should be connected to the ground plane at L3 separately to prevent from ground noise. It should **NOT** be merged with other ground traces, pads, or planes except L3 of PCB.



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MT6236 BT Layout Guideline (2/2)

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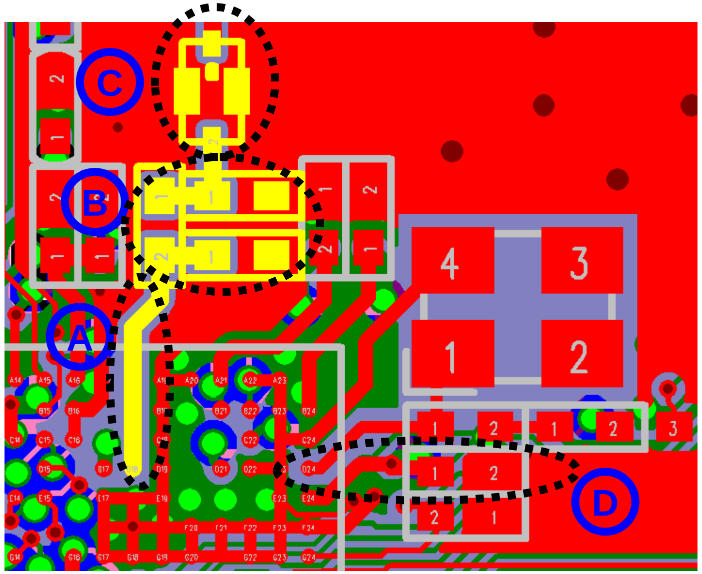
- RF/Analog Part :
  - A. The line width and ground layer reference for RF traces should be kept for better impedance control, which **is close to 50ohm line.**
  - B. The matching BOMs should be placed **as close to chip as possible** for better RF performance.
  - C. Using **qualified** the BPF which is single-in and single-output.
- Power Line Part :
  - D. The routing and decoupling capacitor for VDD28_OSC should be **routed perpendicular to the RF trace.** For other decoupling cap. should be place as close to chip as possible.
  - E. Kept the star-connection for VBT.
- 26MHz Clock :
  - F. The clock trace **MUST** keep as short as possible.
  - G. If using co-clock with RF, the clock trace **MUST** be shielded by GND planes.



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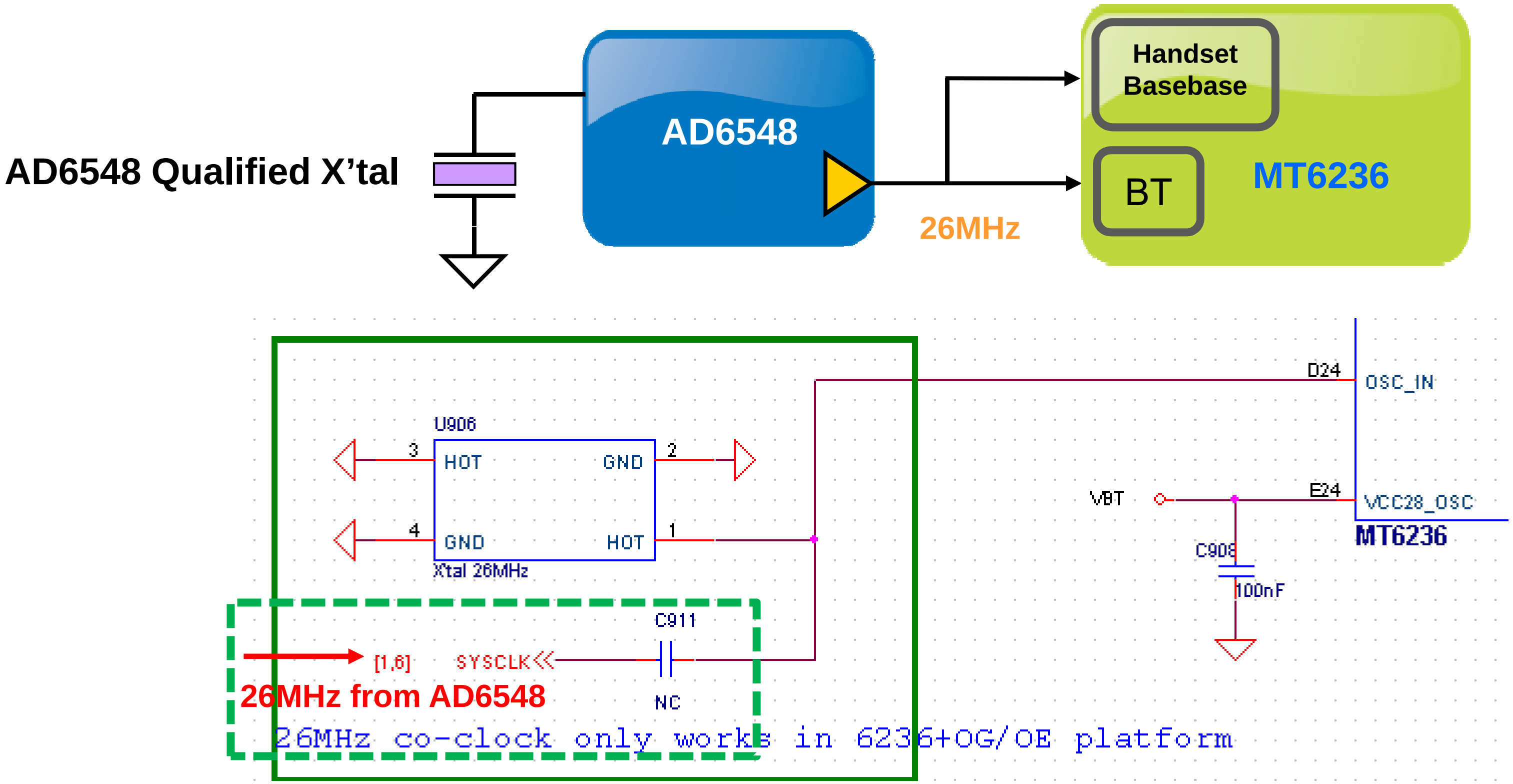
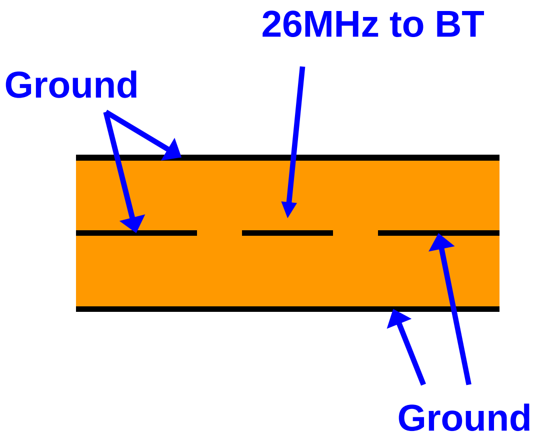
MT6236 BT External Clock Sharing

- MT6236 BT has two options for system clock source.
  - The one is for one-pin crystal input
  - The other is for external clock input **(Only for AD6548/46)**
- The clock source selection can be controlled by on host side.



Special Notes for AD6548 Co-clock Layout

- Follow original design rule for OG and BT if not mentioned.
- 26MHz trace routing rule
  - **As short as possible (Important !)**
  - Good shielding with ground to avoid noise & coupling
- Transceiver trace routing rule
  - Have VCXO power good decouple and clean ground.
- Using MTK recommended OG Xtal
- Reserve BT X'tal footprint for backup.



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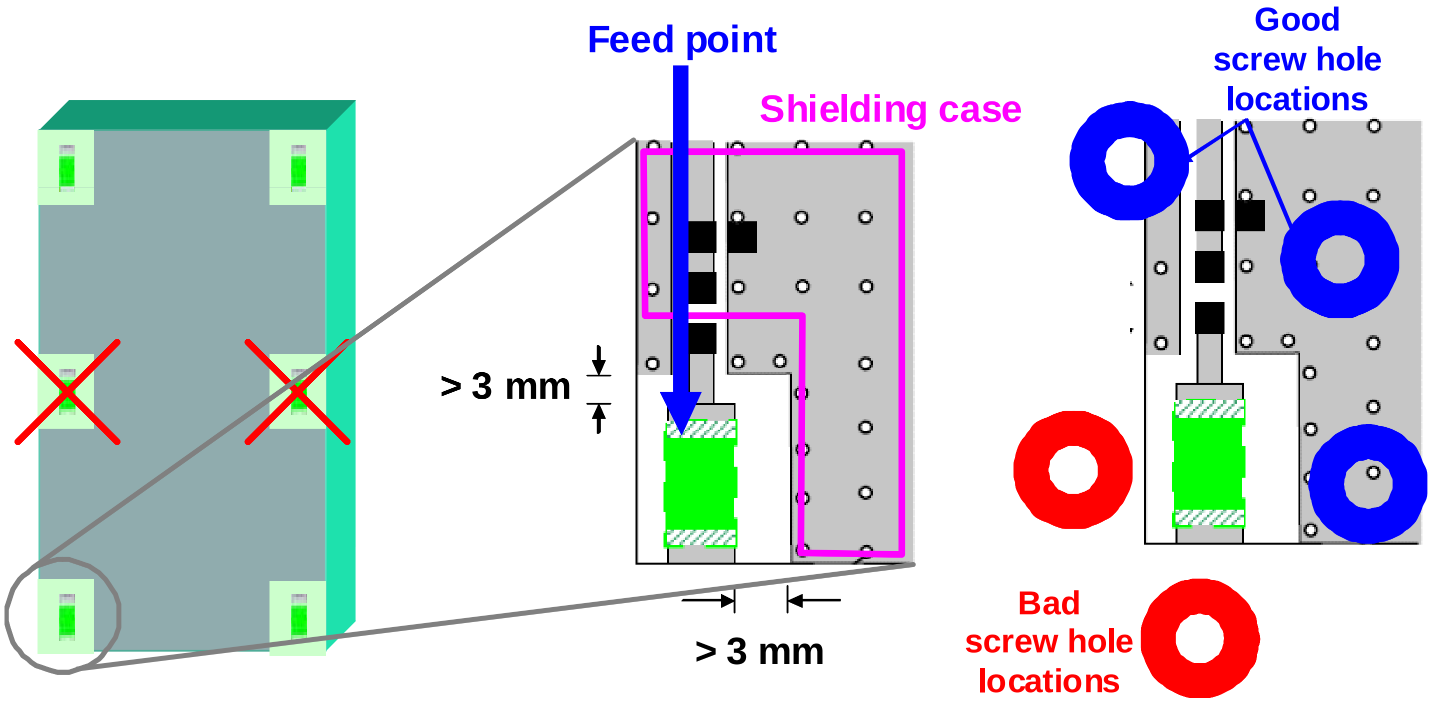
BT Antenna Placement Guideline

- Place the BT antenna at the corner of the PCB.
- The feed point is directly connected to the antenna.
- Reserve enough distance between the antenna, ground and the shielding case.
- Ground blue screw holes, and don't ground red screw holes.



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Design Notice - USB

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Design Notice – USB (1/10)

- **USB 2.0 Test Result :**

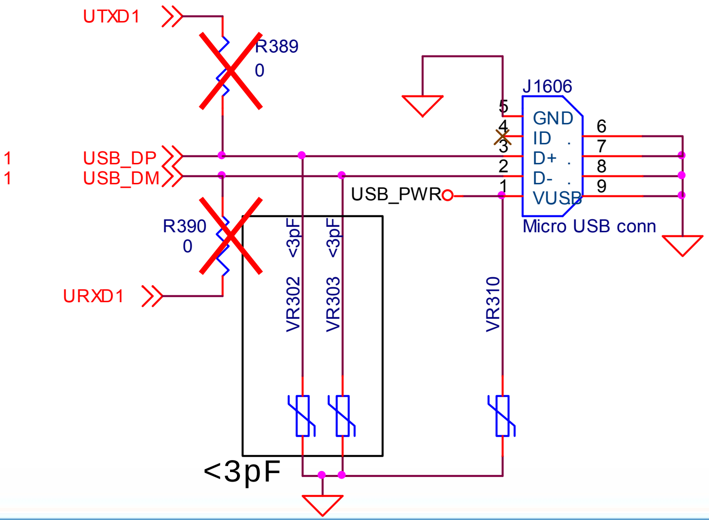
(1) USB2.0 Full Speed : PASS

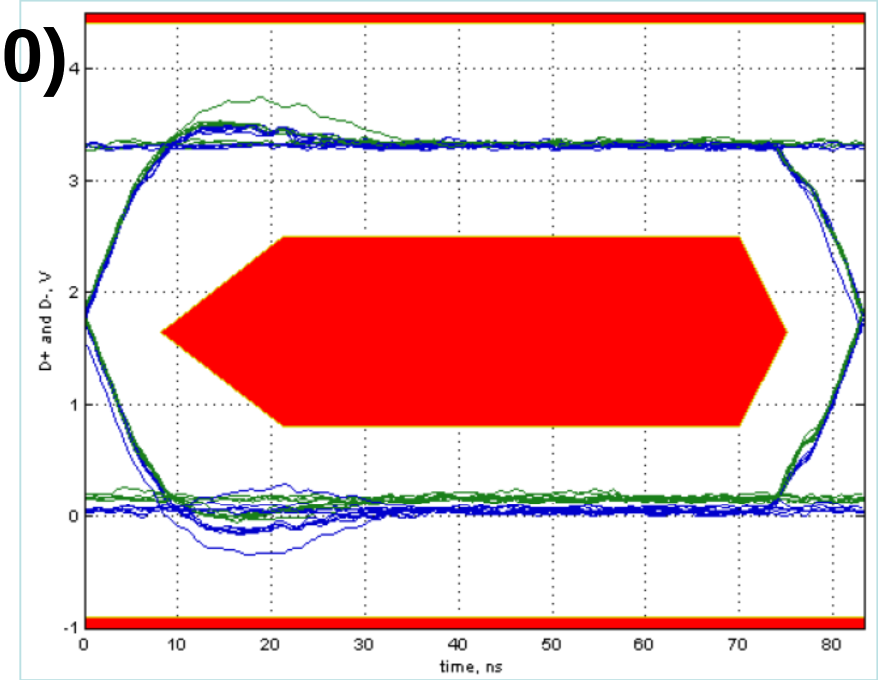
(2) USB2.0 High Speed :

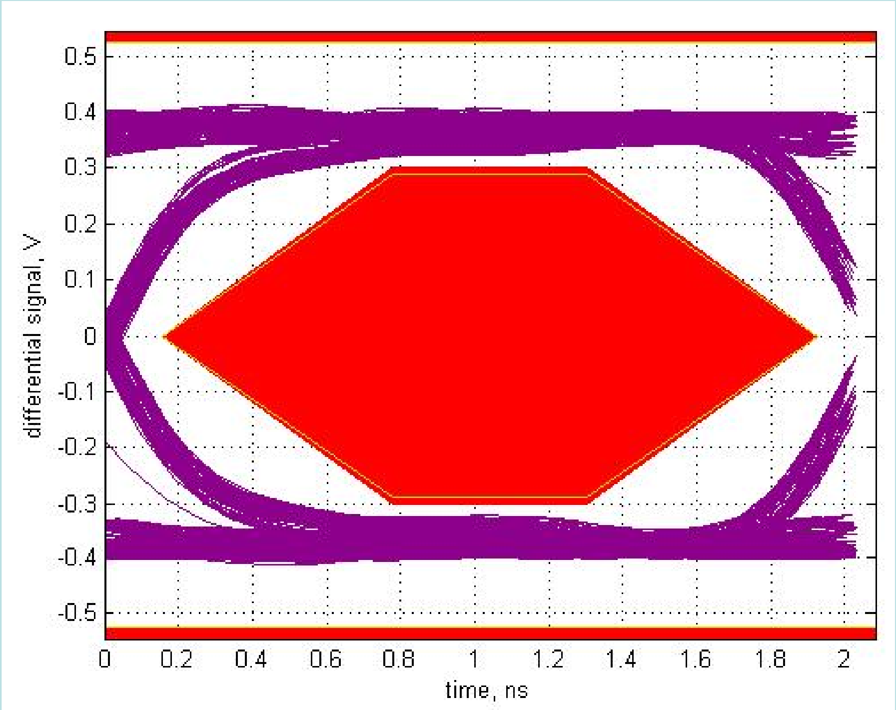
PASS without R389, R390

(R389, R390 will impact USB2.0 test,

please remove R389, R390 during USB testing)







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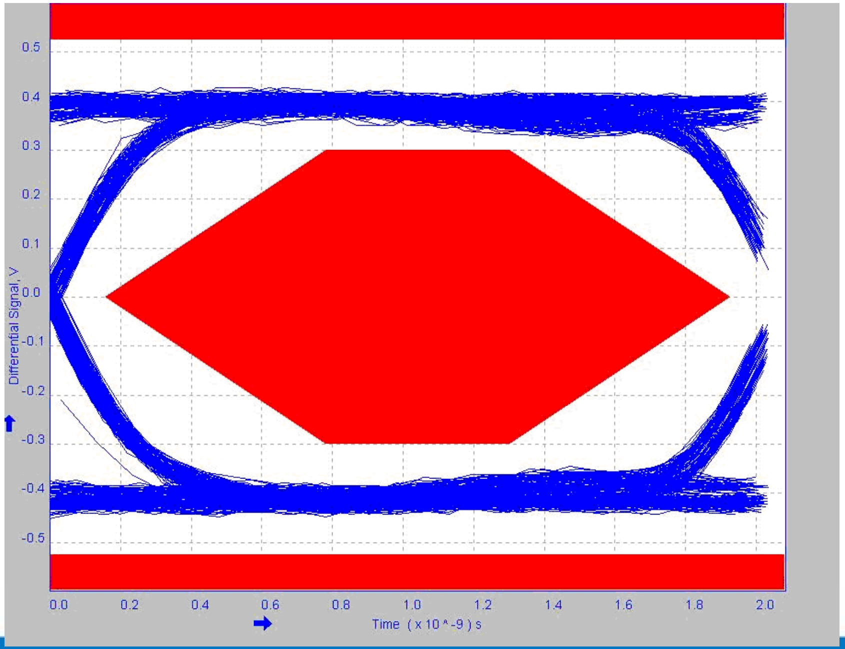
Design Notice – USB (2/10)

- **MTK USB2.0 Solution Introduction**
  - This document introduces MTK USB2.0 design and some points for attention.
    - MTK USB2.0/ OTG device can operate at USB2.0 High-Speed (HS) mode (480Mb/s) and Full-Speed (FS) mode (12Mb/s).
  - General HS eye diagram is shown as below. The output swing is differential 0.4V. Bad eye diagram will lead to certification fail or signal integrity problem.



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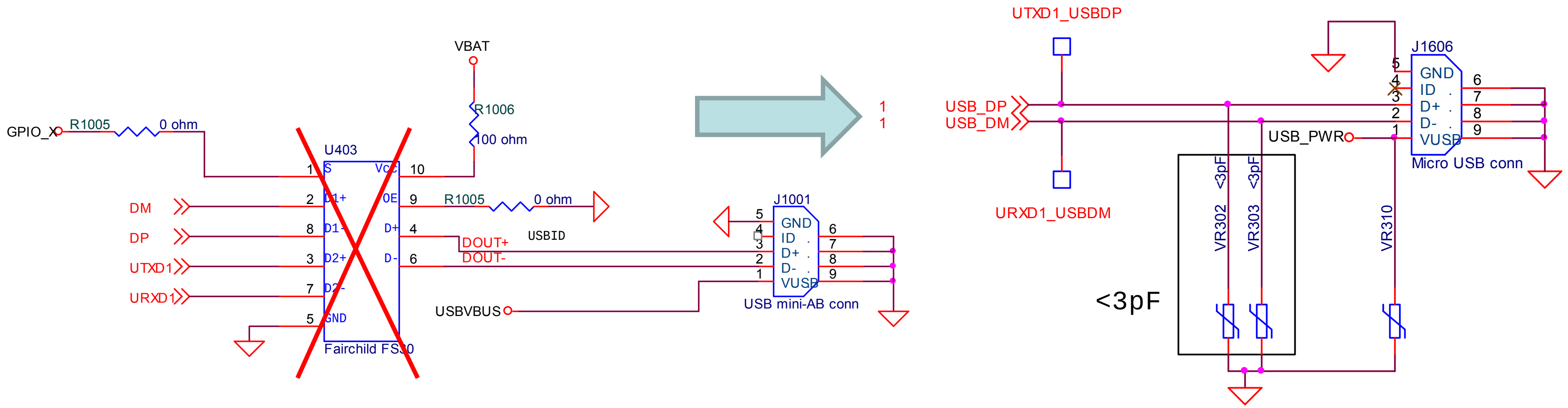
Design Notice – USB (3/10)

- **USB / UART share-pad**
  - MT6236 implement USB_DP/DM & UART1 TX/RX share-pad , power domain = AVDD33_USB (3V3)
    - Advantage : Don't need to add analog switch to switch USB and UART1 path while using MicroUSB connector.
  - In BootROM stage, this share-pad will switch to UART1 TX/RX for flash tool communication. After booting, software will switch this share-pad to USB_DP/DM.



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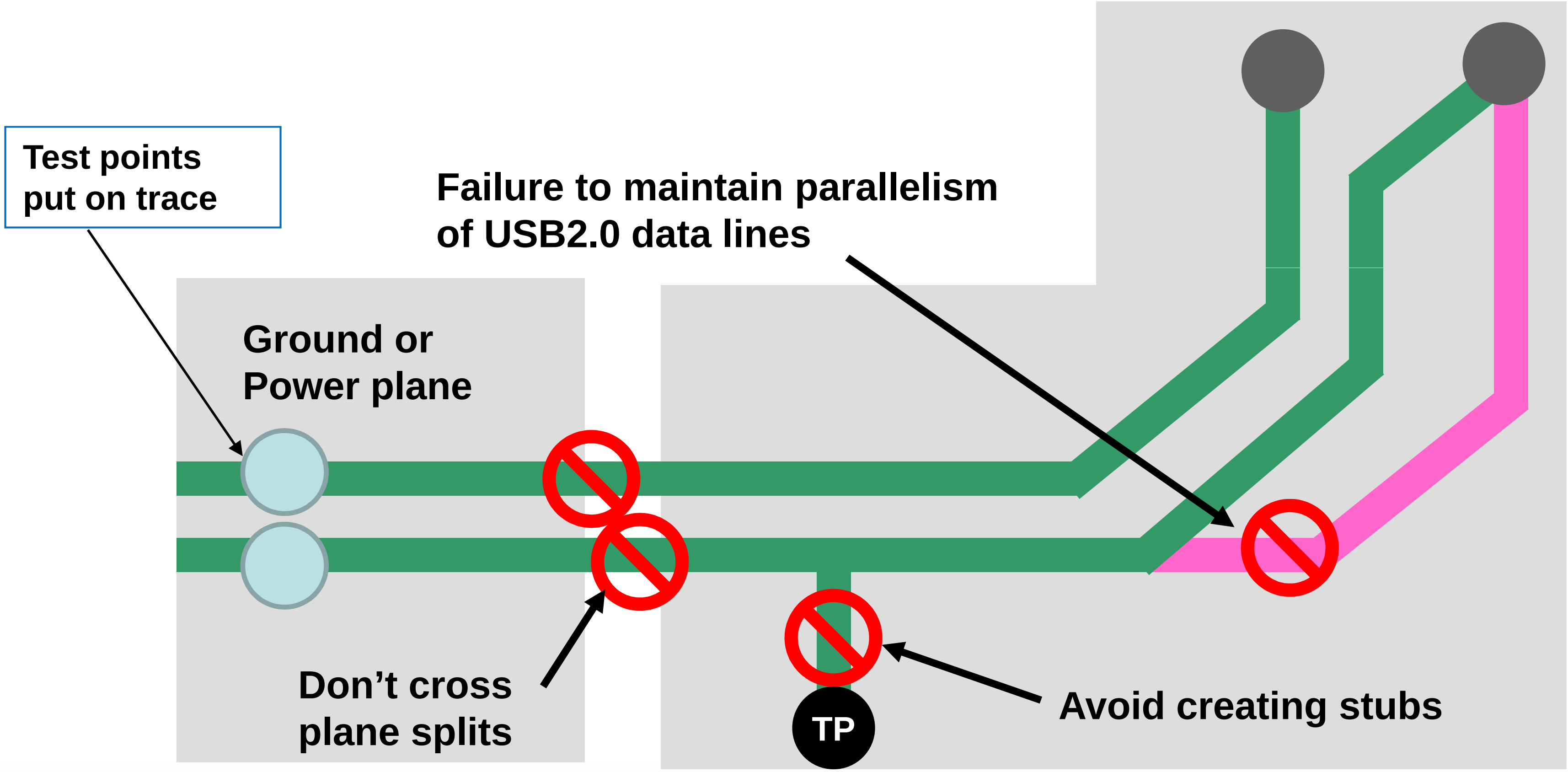
Design Notice – USB (4/10)

- **USB / UART share-pad**
  - If you are using test fixture and need test point on UART TX/RX, please left test point on USB trace or keep dispatch to test point < 10mil



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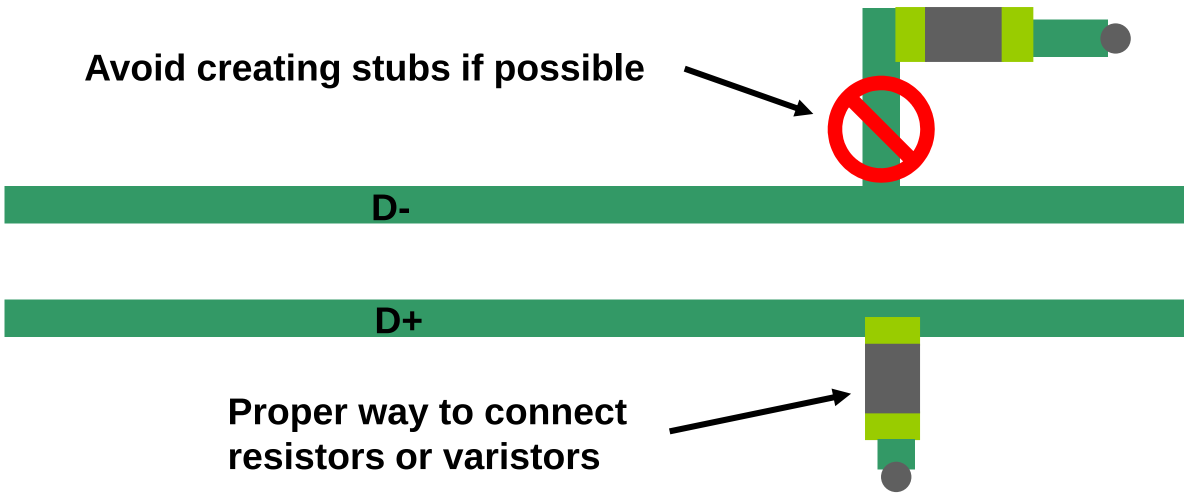
Design Notice – USB (5/10)

- **About Stubs**
  - Avoid creating unnecessary stubs on USB data lines, if a stub is unavoidable (for example: ESD issue), please keep the stub as short as possible.



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Design Notice – USB (6/10)

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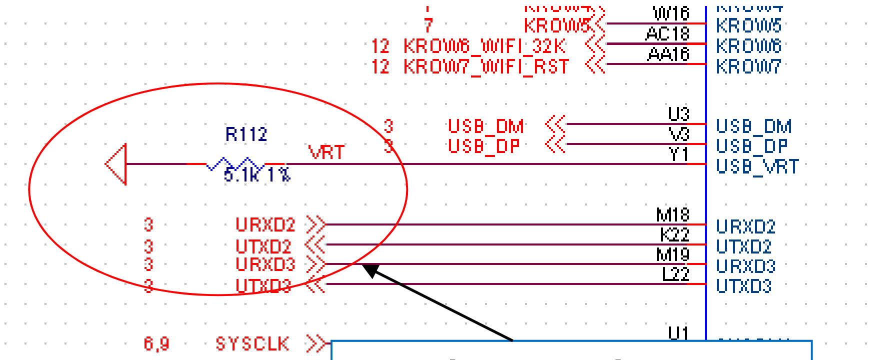
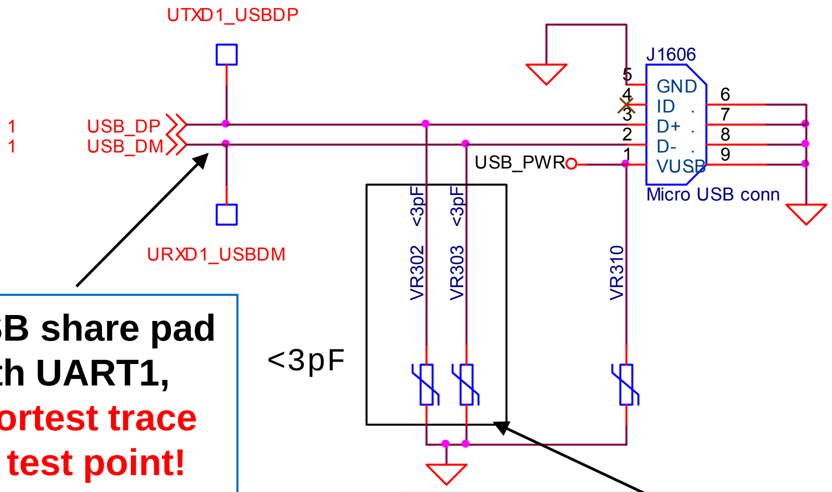
- **USB schematic notice**

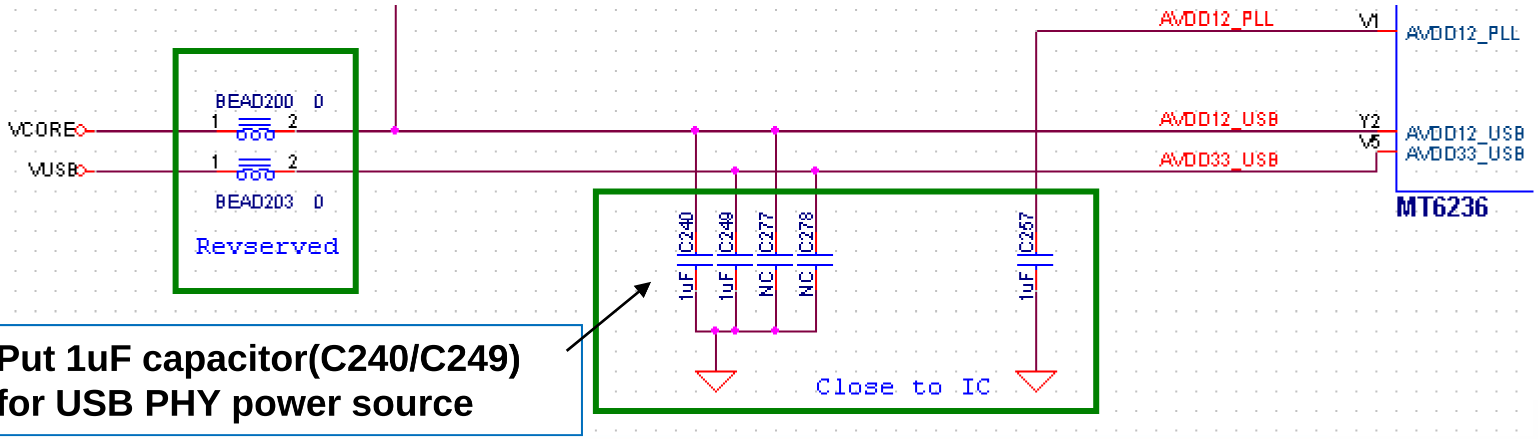


Must be 5.1K ohm, 1%
Place close to IC



USB share pad with UART1, shortest trace on test point!
DP/DM 90 ohm differential

TVS on DP/DM < 3pF for USB 2.0 high speed



Put 1uF capacitor(C240/C249) for USB PHY power source

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Design Notice – USB (7/10)

- **USB 1.1 Full Speed Application**

You can change following make file to support USB 1.1 Full Speed only

- Disable USB 2.0 High Speed Support at make file

  USB2.0_HS_SUPPORT = FALSE # TRUE, FALSE
  # True to enable USB High Speed

The loading for USB 1.1 full speed should follow Universal Serial Bus Specification 7.1.2, <50pF

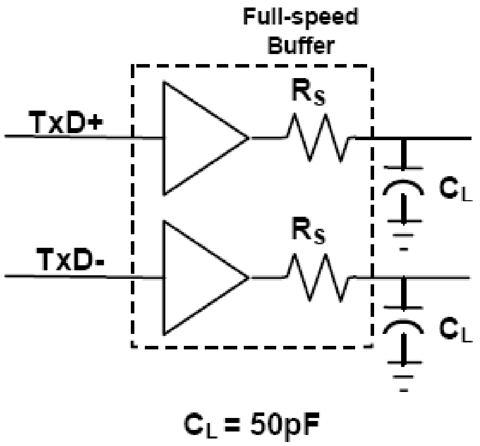

Figure 7-7. Full-speed Load

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Design Notice – USB (8/10)

- **USB-IF Certification**
  - To pass dead battery pre-connect current on USB ECN, have to larger the 0.2 ohm Rsense on charger to reduce pre-charge current under 100mA.

USB ENGINEERING CHANGE NOTICE

Title: **USB 2.0 Connect Timing**

Applies to: **Universal Serial Bus Specification, Revision 2.0**

Summary of ECN

This ECN addresses the following three issues:

- dead battery pre-connect current
- post-connect current timing
- VBUS valid to connect timing

Dead battery pre-connect current

The Battery Charging spec contains the Dead Battery Provision, which allows devices with weak or dead batteries to draw up to 100mA for the time required to power the device up, and bring it to a state where it can connect.

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Design Notice – USB (9/10)

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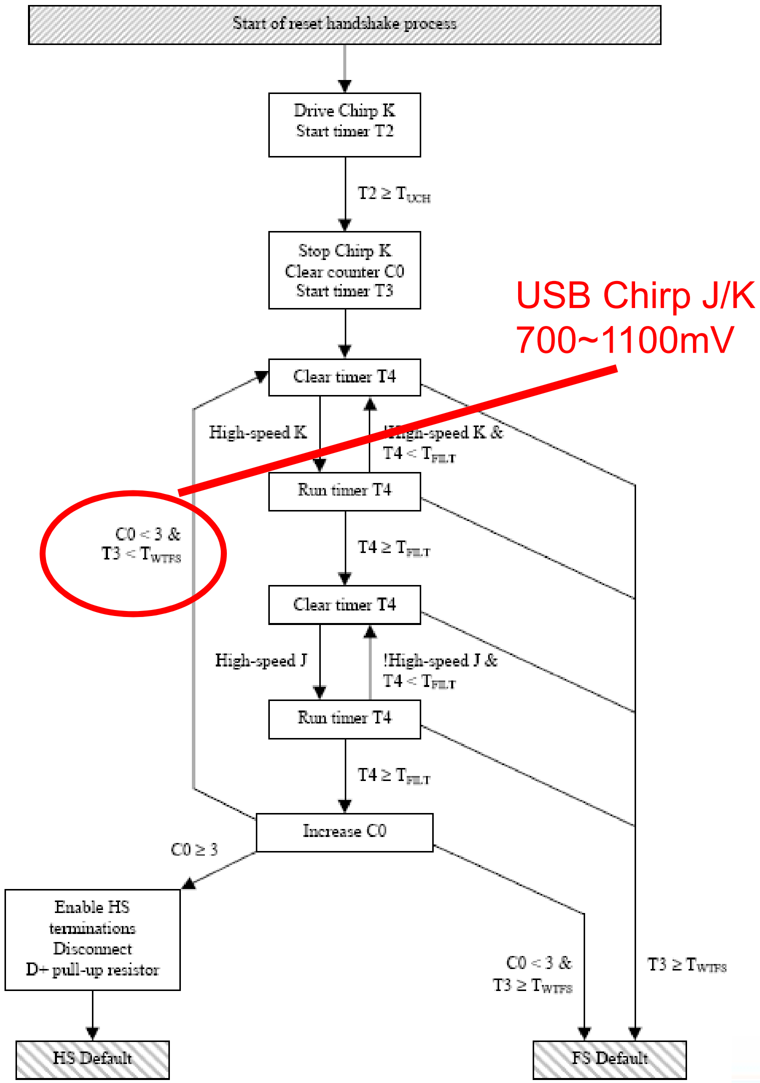
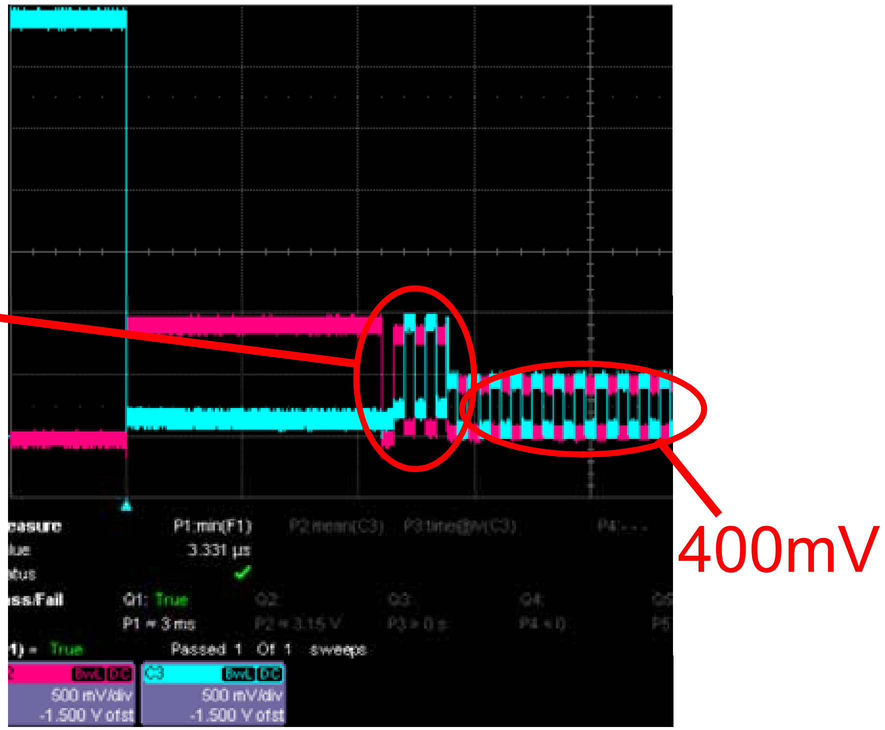
- **USB HS/FS Mode Handshake** (Due to USB2.0 SCH/Layout are both critical, please refer to "MTK_USB_Application_Notes" to get more information)





- Bad cable or layout may cause pass handshake and enable HS mode but fail transmission due to too much CRC error.
- Can't implement auto switch HS/FS mode at device side.

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Design Notice – USB (10/10)

- **Mediatek USB 2.0 High Speed Service Notice**

  - Mediatek strongly suggest customer use USB connectors compliance with Mini USB or Micro USB standard.
    - Mediatek provide USB 2.0 high speed signal quality test service if using Mini USB or Micro USB connector.
    - Will checked by qualified USB cables.
  - We can't guaranty USB 2.0 high speed connection and quality if using non-standard connector (18-pin, 12-pin etc) and cables.
    - Suggest to configure it as full speed mode. (compile option)

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Design Notice – Audio/Speech

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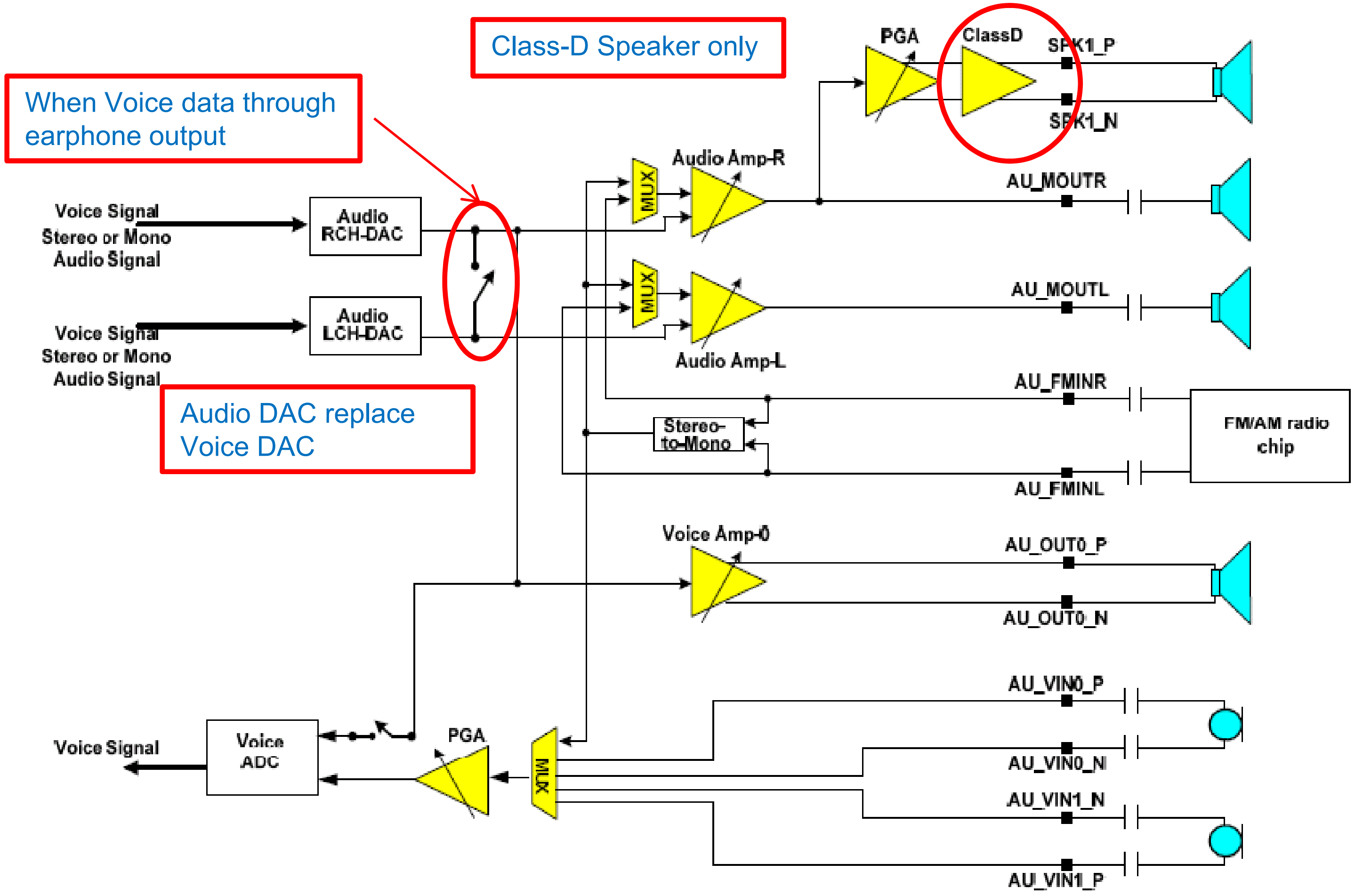
Design Notice – Audio (1/9)

- **Audio Block diagram :**



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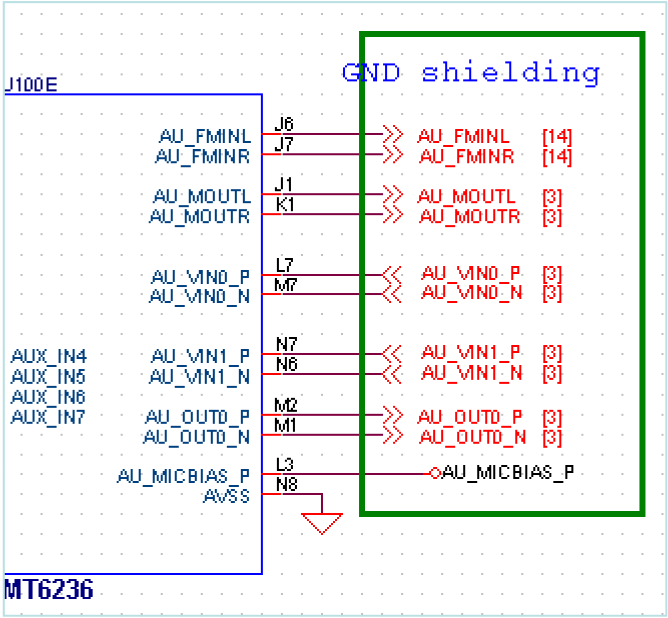
Design Notice – Audio (2/9)

- **Audio Signal schematic and layout :**
  - The signal of Audio block should shielding by GND



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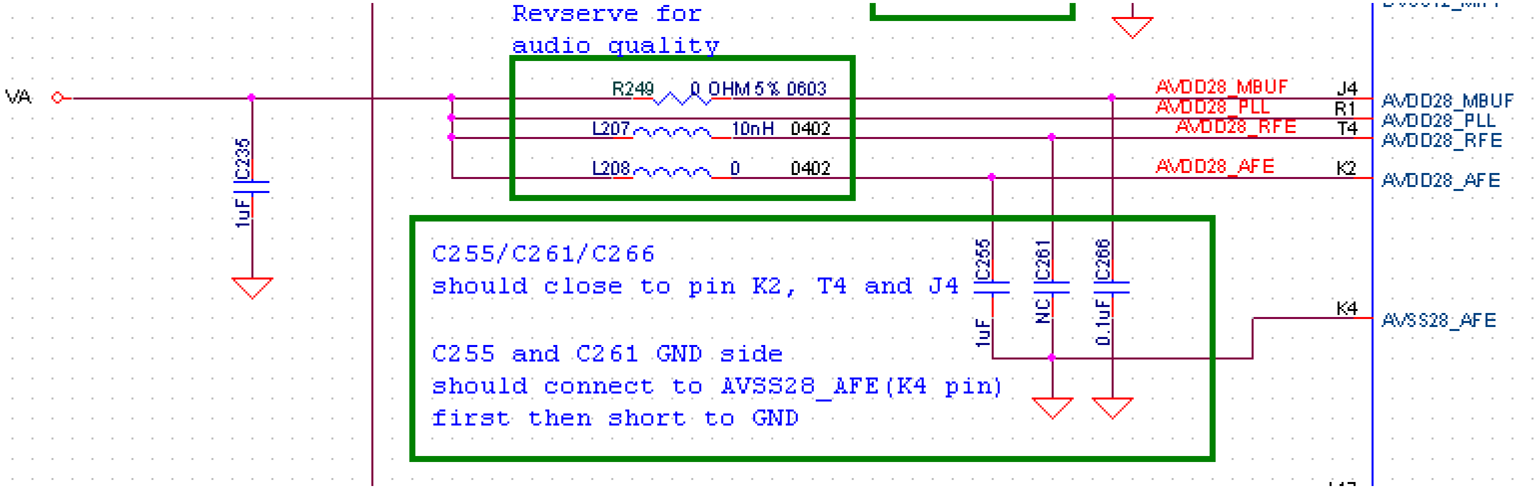
Design Notice – Audio (3/9)

- **Audio Power schematic and layout :**
  - C255 and C261 GND side should connect to AVSS28_AFE first then short to GND
  - C255, C261, C266 should close to ball K2, T4 and J4



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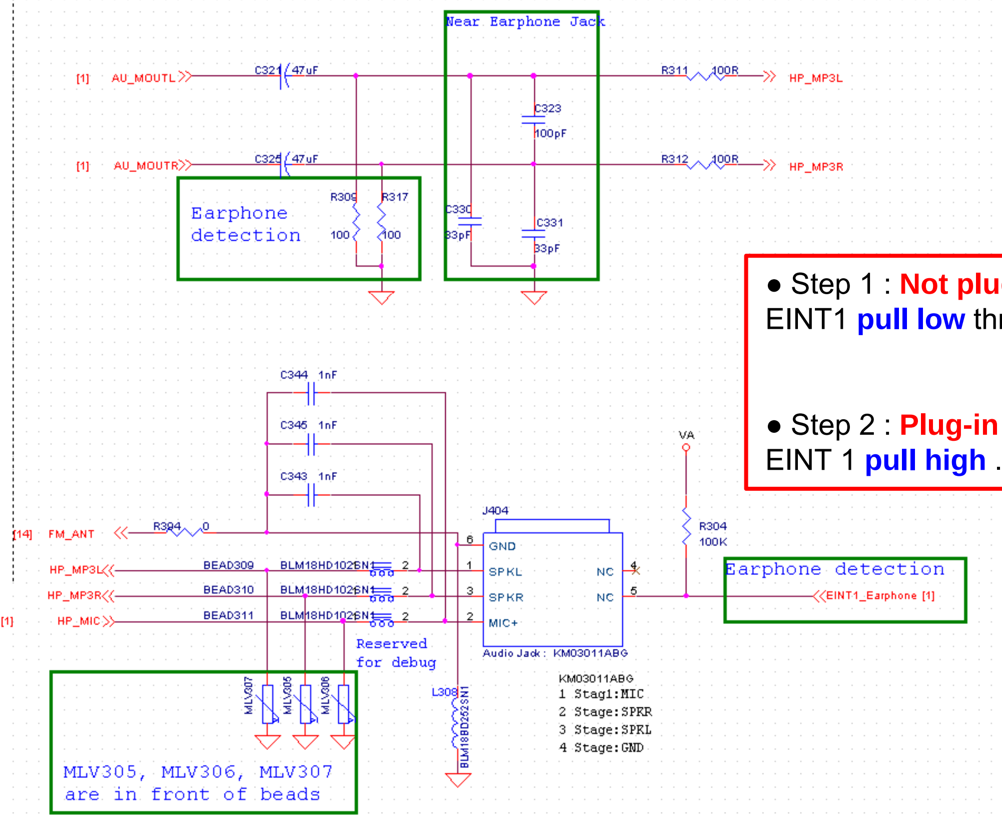
Design Notice – Audio (4/9)

- **Audio Jack :**
  - An extra interrupt pin of audio jack for the earpiece detection can get better THD+N (from 71dB to 76dB)

Earphone Receiver



● Step 1 : **Not plug-in** earphone (Audio Jack pin 3-5 connected)
EINT1 **pull low** through Audio Jack (pin 3-5 connection) to R317 to GND.

● Step 2 : **Plug-in** earphone (Audio Jack pin 3-5 dis-connected)
EINT 1 **pull high** .

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Design Notice – Audio (5/9)

- **Audio Jack :**
  - In previous page, EINT status is from **Low**(earphone plug out) to **High** (earphone plug-in), so please confirm auxmain.c to fit hardware application

•Example for EINT status is from Low (plug out) to High (plug-in)

```
kal_bool            aux_state = LEVEL_LOW;
                    :
                    :
void AUX_EINT_HISR(void)
{
ilm_struct *aux_ilm;

 if (aux_state == LEVEL_HIGH)
 {
  #ifdef AUX_DEBUG
dbg_print(" Interrupt: Plugout \n\r");
 #endif
```

•Example for EINT status if from High (plug out) to Low (plug in)

```
kal_bool            aux_state = LEVEL_HIGH;
                    :
                    :
void AUX_EINT_HISR(void)
{
 ilm_struct *aux_ilm;

 if (aux_state == LEVEL_LOW)
 {
 #ifdef AUX_DEBUG
dbg_print(" Interrupt: Plugout \n\r");
#endif
```

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Design Notice – Audio (6/9)

- **Internal Class-D : Audio Amplifier Power Output**

	MT6236 Class-D Amplifier	
Pomax Maximun output power	THD+N=10%, VDD=4.2V RL = 8 Ω	1.0W
	THD+N=10%, VDD=3.3V RL = 8 Ω	650mW
	THD+N=1%, VDD=4.2V RL = 8 Ω	850mW
	THD+N=1%, VDD=3.6V RL = 8 Ω	500mW

- Although MT6236 class-D power output is 0.85W at 8 Ω , because congenital power source limitation is 4.2V from VBAT , but compare with other discrete amplifiers , MT6236 equal other amplifier in performance.

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Design Notice – Audio (7/9)

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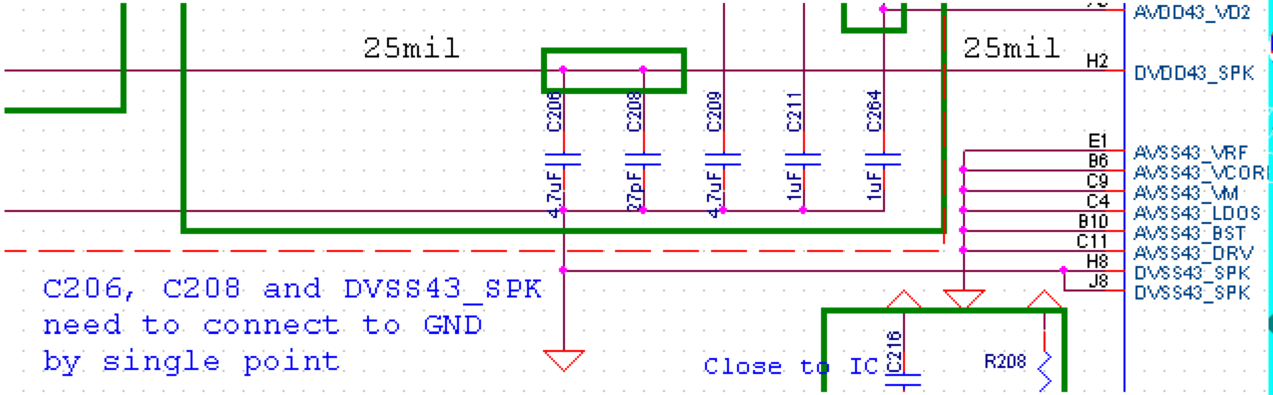
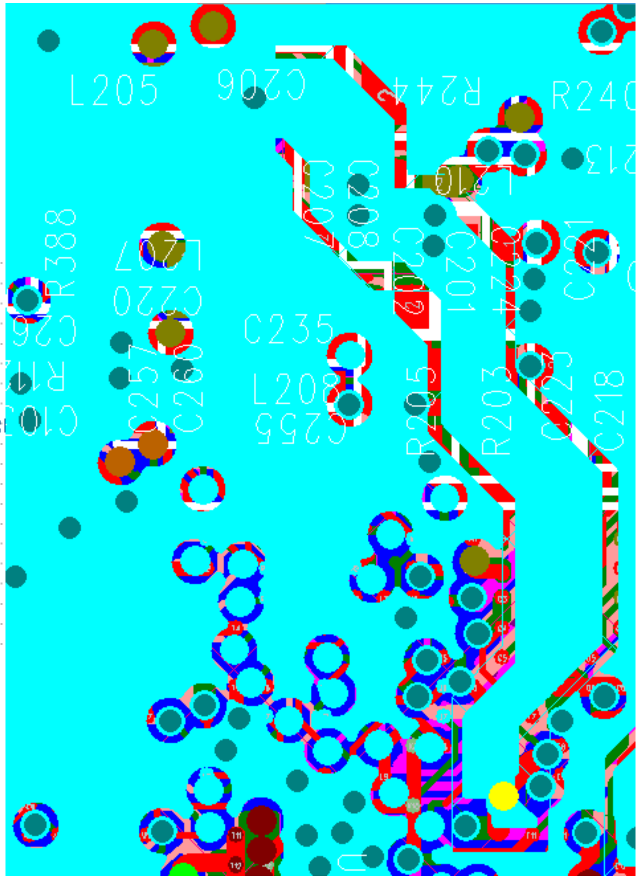
- **Internal Class-D Audio Amplifier :**
  - C206, C208 and DVSS43_SPK need to connect to GND by single point





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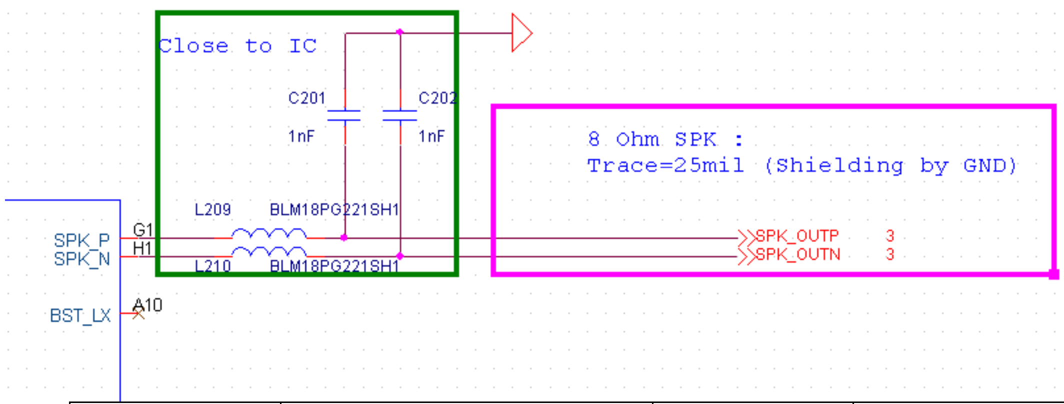
Design Notice – Audio (8/9)

Confidential B

- **Internal Class-D Audio Amplifier :**
  - The placement of L209 and L210 should be closed to MT6236
  - The trace width of SPK_P and SPK_N should be greater than 25 mil
  - The Net of SPK_P and SPK_N should be shielded by GND
  - Please select Bead for Amp output filter which R_{DC} < 0.1ohm and Rated Current > 1.1A



Vendor	P/N	Rdc(ohm)	Rate current(mA)
Murata	BLM18PG221SH1	0.1	1400
	BLM15PD800SN1	0.07	1500
	BLM18KG221SN1	0.05	2200
	BLM18KG331SN1	0.08	1700
	BLM18SG221TN1	0.04	2500
	BLM18SG331TN1	0.07	1500
	BLM18EG221SN1	0.05	2000
TDK	MPZ1608S221A	0.05	2200
	MPZ1608S331A	0.08	1700
	MPZ1608Y221B	0.1	1500

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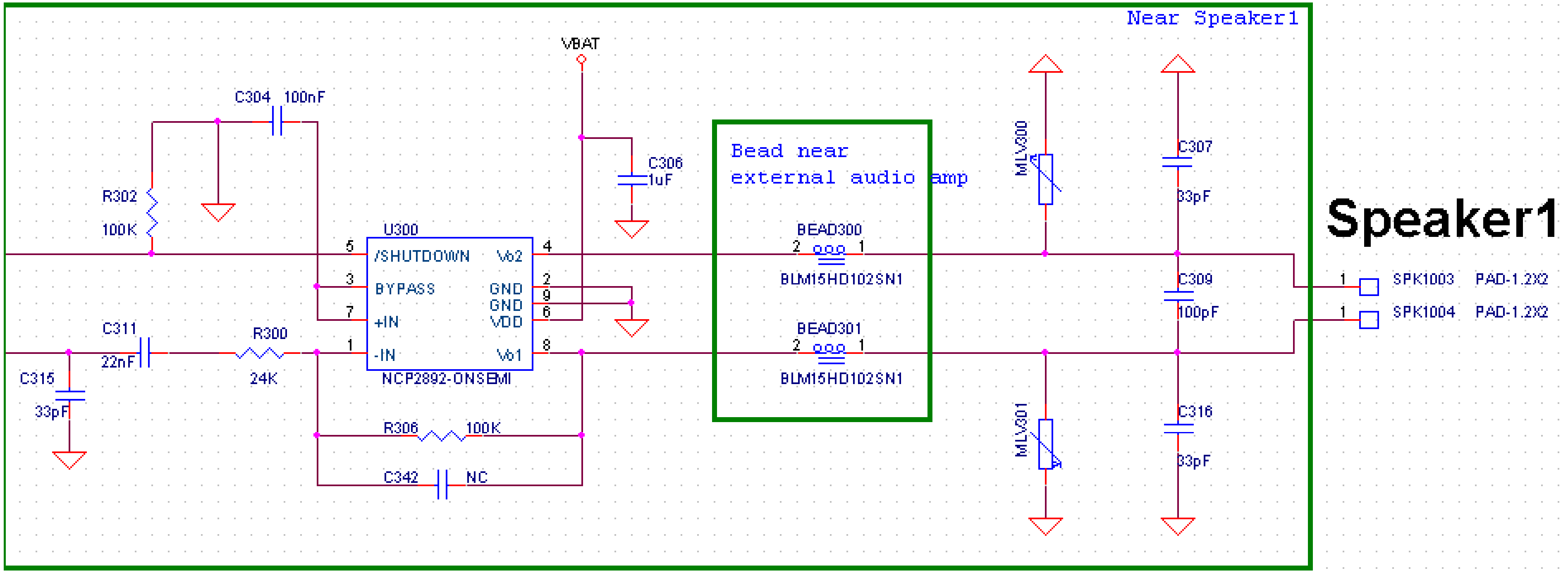
Design Notice – Audio (9/9)

- **External audio amplifier :**
  - When use the external audio amp for stereo application, place the amp close to speaker.
  - Bead300 and Bead301 should be close to external audio amp



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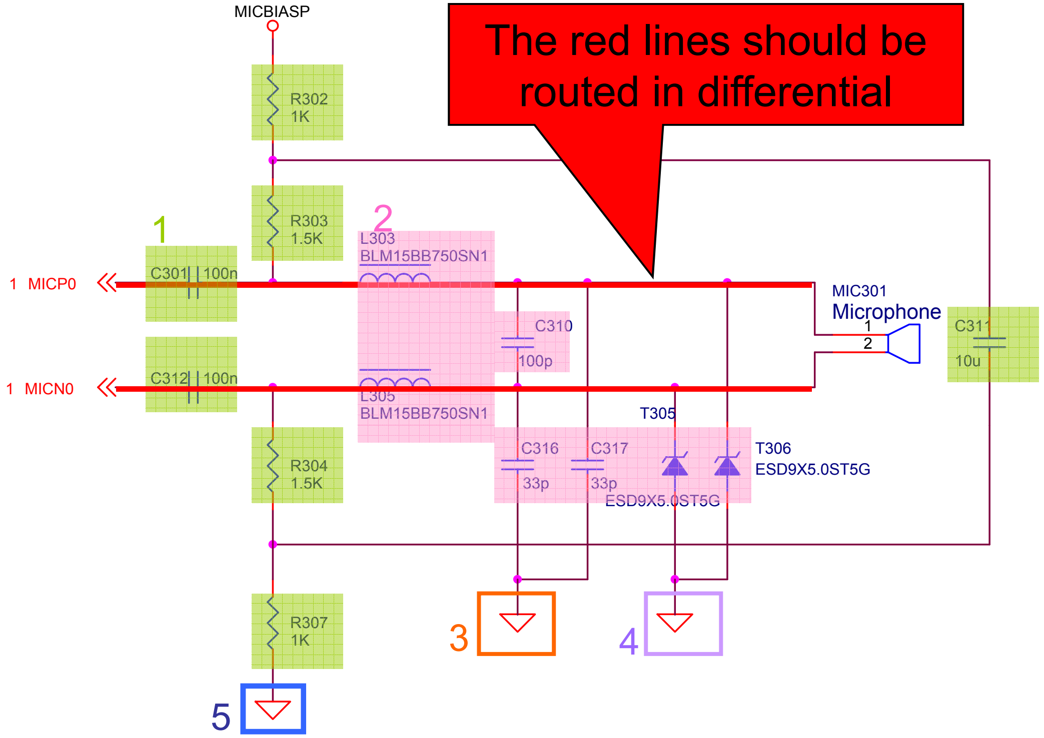
Design Notice – Speech (1/3)

- **Application for the Differential circuit :**
  - Layout consideration-Normal mode



1. R302, R303, R304, R307, C311, C301 and C312 should be put **close to the BB chip**
   – R302, R303, R304, R307, C311 should be put as close as possible
2. L303, L305, C310, C316, C317, T305 and T306 should be **close to the microphone**
3. GND of **C316 and C317** should be connected **together** and then to the GND
4. GND of **T305 and T306** should be connected **together** and then to the GND
5. GND of **R307**should connect to the **main GND by a single via**

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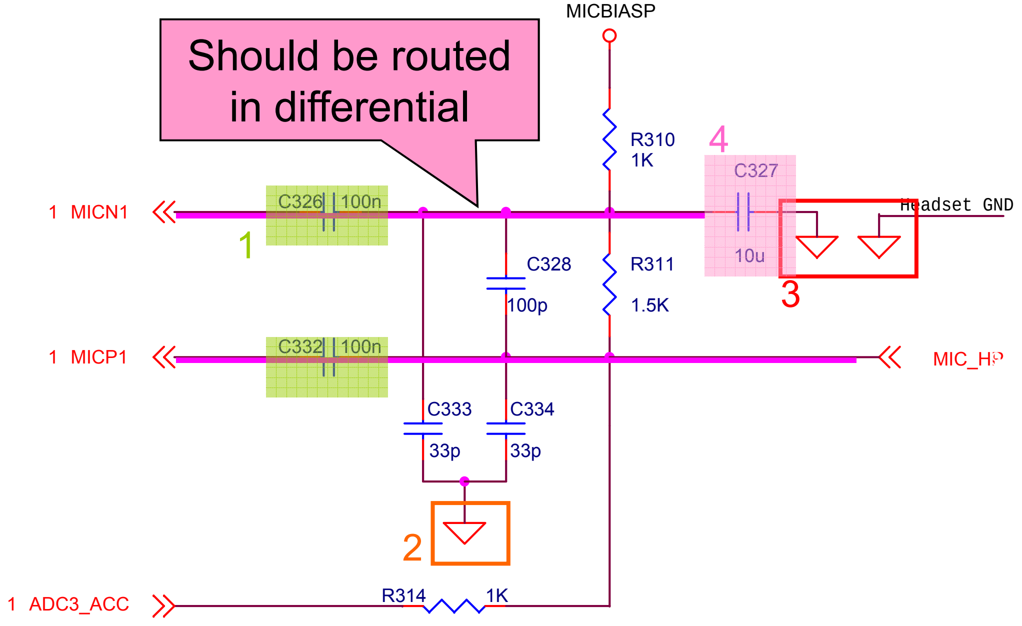
Design Notice – Speech (2/3)

- **Application for the Differential circuit :**

  - Layout consideration-Headset mode



1. **C326, C332, R311, R310** should be put **close to BB**
2. The **GND of C333 and C334** should **connect together and then connect to the GND**
3. The **GND of C327 and headset** should **connect together and then to the main GND by single via**
4. **C327** should be put **close to microphone**

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Design Notice – Speech (3/3)

- **Key placement and grounding rule to assure the UL performance:**

  - The placement and grounding of following capacitors should be taken care well

	Capacitor between	Layout rule
MT6253	AU_VCM	1. Put them **as close as possible** to the pads 2. Connect the GND of these caps to the **main GND** instead of the ground at the top / bottom layer
MT6516 / MT6268	AU_VCM_PO / NO	
MT6236 and other projects afterwards	VREF (Bandgap output)	

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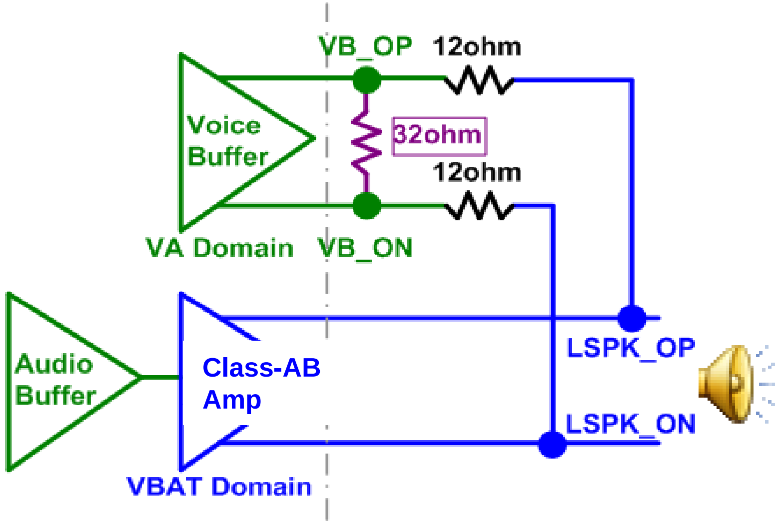
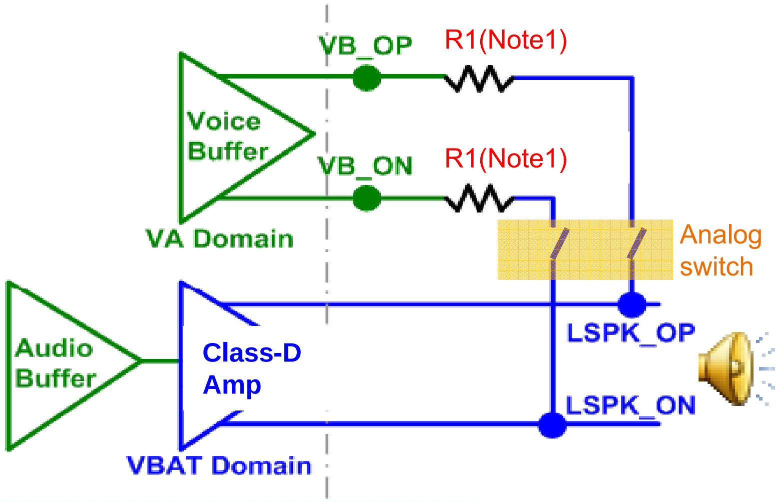
Notice for 2-on-1 speaker application

- Class-AB (external amp)
  - **Adding one "32ohm" between (VB_OP, VB_ON)** to limit the voltage level at (VB_OP, VB_ON)



- Class-D **(MT6236 build-in** or external amp**)**
  - **"2 analog switches"** should be put **between VB_OP/ON and LSPK_OP/ON**
  - **Note1: The R1+Ron of the analog switch should equal to 12ohm**



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Design Notice – GPIO Selection

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Design Notice – GPIO selection (1/8)

1. Pull-Up / Pull-Down selection :

- Choose GPIO with suitable PU/PD after reset state for application
  - Ex : As for "enable pin of audio amplifier", please choose GPIO with **PD** after reset state
  - Ex : As for "enable pin of external LDO", please choose GPIO with **PD** after reset state

2. Power domain of IO supply selection :

- Choose GPIO with suitable power domain of IO supply for application
  - GPIO [0:9] DVDD28
  - GPIO [10:13] DVDD_MC2
  - GPIO [14:17] DVDD_KP
  - GPIO [18:30] DVDD_CAM
  - GPIO [31:38] DVDD_NFI
  - GPIO [39:40] DVDD28
  - GPIO [41] DVDD_NFI
  - GPIO [42:46] DVDD28
  - GPIO [47:51] DVDD_PCM
  - GPIO [52:64] DVDD28
  - GPIO [65:67] VSIM2

3. Please choose suitable GPIO for peripheral IC :

- Please choose GPIOs with matched direction, pull-up/pull-down, data inversion, data output, gpio mode after reset state for peripheral IC application

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Design Notice – GPIO selection (2/8)

Confidential B

- Yellow area is the reset state of "GPIO mode" and "PU/PD" (refer to datasheet chapter 4.4)
- GPIO [10:13] will be workable after DVDD_MC2 (ball C14) active

Ball	Name	Default Mode	Mode 0	Mode 1	Mode 2	Mode 3	Default PU/PD	Power domain	Voltage	Schmitt Trigger	Buffer
			Function	Function	Function	Function					strength
RF Parallel Control Unit											
AA3	BPI_BUS0	0	GPIO0	BPI_BUS0			PD	DVDD28	2.8V	No	2,4,6,8
AD3	BPI_BUS1	0	GPIO1	BPI_BUS1			PD	DVDD28	2.8V	No	2,4,6,8
AA4	BPI_BUS2	0	GPIO2	BPI_BUS2			PD	DVDD28	2.8V	No	2,4,6,8
AB4	BPI_BUS3	0	GPIO3	BPI_BUS3			PD	DVDD28	2.8V	No	2,4,6,8
AA5	BPI_BUS4	0	GPIO4	BPI_BUS4			PD	DVDD28	2.8V	No	2,4,6,8
AC4	BPI_BUS5	0	GPIO5	BPI_BUS5			PD	DVDD28	2.8V	No	2,4,6,8
Y6	BPI_BUS6	0	GPIO6	BPI_BUS6			PD	DVDD28	2.8V	No	2,4,6,8
AB5	BPI_BUS7	0	GPIO7	BPI_BUS7			PD	DVDD28	2.8V	No	2,4,6,8
Y7	BPI_BUS8	0	GPIO8	BPI_BUS8	CLKM0	MC0INS	PD	DVDD28	2.8V	No	2,4,6,8
AD4	BPI_BUS9	0	GPIO9	BPI_BUS9			PD	DVDD28	2.8V	No	2,4,6,8
SPI Interface											
G14	SPI_CS_N	0	GPIO10	SPI_CS_N	MC1CM0	MC0DA7	PU	DVDD_MC2	1.8V/2.8V/3.3V	No	2,4,6,8,10,12,14,16
G13	SPI_SCK	0	GPIO11	SPI_SCK	MC1DA0	MC0DA6	PU	DVDD_MC2	1.8V/2.8V/3.3V	No	2,4,6,8,10,12,14,16
F13	SPI_MOSI	0	GPIO12	SPI_MOSI	MC1CK	MC0DA5	PU	DVDD_MC2	1.8V/2.8V/3.3V	No	2,4,6,8,10,12,14,16
F12	SPI_MISO	0	GPIO13	SPI_MISO	MC1DA1	MC0DA4	PU	DVDD_MC2	1.8V/2.8V/3.3V	No	2,4,6,8,10,12,14,16

- The power domain of GPIO [10:13] is DVDD_MC2.
For Mode 0/1, please connect DVDD_MC2 (ball C14) to VIO (ball B5)
For Mode 2, please connect DVDD_MC2 to external LDO
For Mode 3, please connect DVDD_MC2 to VMC (ball E8)

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Design Notice – GPIO selection (3/8)

- Yellow area is the reset state of "GPIO mode" and "PU/PD" (refer to datasheet chapter 4.4)
- GPIO [14:17] will be workable after DVDD_KP (ball AB17) active
- GPIO [18:30] will be workable after DVDD_CAM (Y19) active

● Generally connect to VIO (ball B5)

Ball	Name	Default Mode	Mode 0 Function	Mode 1 Function	Mode 2 Function	Mode 3 Function	Default PU/PD	Power domain	Voltage	Schmitt Trigger	Buffer strength
Keypad Interface											
AC15	KCOL7	0	GPIO14	KCOL7	EDICK	LPCE2B	PU	DVDD_KP	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AD16	KCOL6	0	GPIO15	KCOL6	EDIWS	BT2WIFI_0	PU	DVDD_KP	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AA16	KROW7	0	GPIO16	KROW7	EDIDAT	URXD3	PD	DVDD_KP	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AC18	KROW6	0	GPIO17	KROW6	CLKM1	UTXD3	PD	DVDD_KP	1.8V/2.8V	No	2,4,6,8,10,12,14,16
CMOS Sensor Interface											
U16	CMRST	0	GPIO18	CMRST	D2_TID0	D1ICK	PD	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AC20	CMPDN	0	GPIO19	CMPDN	D2_TID1	D1ID	PD	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
W18	CMVREF	0	GPIO20	CMVREF	CLKM3	D1IMS	PD	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AB18	CMHREF	0	GPIO21	CMHREF	D1_TID0	D2ICK	PD	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
U17	CMPCLK	0	GPIO22	CMPCLK	D1_TID1	D2ID	PD	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
Y18	CMMCLK	0	GPIO23	CMMCLK	DEBUG0	D2IMS	PD	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AA18	CMDAT9	0	GPIO24	CMDAT9	DEBUG1	TDTIRQ	PD	DVDD_CAM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
AB19	CMDAT8	0	GPIO25	CMDAT8	DEBUG2	TCTIRQ1	PD	DVDD_CAM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
V18	CMDAT7	0	GPIO26	CMDAT7	DEBUG3	TBTXEN	PD	DVDD_CAM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
AC21	CMDAT6	0	GPIO27	CMDAT6	DEBUG4	TBTXFS	PD	DVDD_CAM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
W19	CMFLASH	0	GPIO28	CMFLASH	DEBUG5	TBRXEN	PD	DVDD_CAM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
Camera Control Interface											
AA19	SCL	0	GPIO29	SCL	DEBUG6	TBRXFS	PU	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
AB20	SDA	0	GPIO30	SDA	DEBUG7	TCTIRQ2	PU	DVDD_CAM	1.8V/2.8V	No	2,4,6,8,10,12,14,16

● Generally connect to VCAMA or VCAMD (should same with Camera device IO power domain)

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Design Notice – GPIO selection (4/8)

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- Yellow area is the reset state of “GPIO mode” and “PU/PD” (refer to datasheet chapter 4.4)
- GPIO [31:38] will be workable after DVDD_NFI (ball T19) active.

● Be careful the power domain of GPIO [31:38]

Ball	Name	Default Mode	Mode 0 Function	Mode 1 Function	Mode 2 Function	Mode 3 Function	Default PU/PD	Power domain	Voltage	Schmitt Trigger	Buffer strength
Serial LCD/PM IC Interface											
Y22	LSA0	0	GPIO31	LSA0	URXD2	CLKM3	PD	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
Y23	LSCK	0	GPIO32	LSCK	UTXD2	CLKM4	PD	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
W20	LSDA	0	GPIO33	LSDA	CAM_STROBE	LPCE2B	PD	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
Parallel LCD/NAND-Flash Interface											
W22	LPCE1B	0	GPIO34	LPCE1B	LSCE0B		PU	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
U19	LPCE0B	0	GPIO35	LPCE0B	LSCE1B		PU	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
V22	LPTE	0	GPIO36	LPTE	CLKM2	TEVTVAL	PD	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
V23	NLD17	0	GPIO37	NLD17	CAM_MECH0		PD	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
W23	NLD16	0	GPIO38	NLD16	CAM_MECH1		PD	DVDD_NFI	1.8V/2.8V	No	2,4,6,8,10,12,14,16
UART/IrDA Interface											
M18	URXD2	0	GPIO45	URXD2	UCTS3	D2_TID2	PU	DVDD28	2.8V	Yes	2,4,6,8
K22	UTXD2	0	GPIO46	UTXD2	URTS3	D2_TID3	PU	DVDD28	2.8V	No	2,4,6,8
M19	URXD3	0	GPIO39	URXD3	UCTS2	D2_TID4	PU	DVDD28	2.8V	Yes	2,4,6,8
L22	UTXD3	0	GPIO40	UTXD3	URTS2	D2_TID5	PU	DVDD28	2.8V	No	2,4,6,8
H23	IRDA_TXD	0	GPIO55	IRDA_TXD	PWM3	TDMA_FS	PU	DVDD28	2.8V	No	4,8,12,16
K20	IRDA_RXD	3	GPIO56	IRDA_RXD	PWM4	UCTS1	PU	DVDD28	2.8V	No	4,8,12,16
J23	IRDA_PDN	3	GPIO57	IRDA_PDN	PWM5	URTS1	PU	DVDD28	2.8V	No	4,8,12,16

● Be careful the reset state of GPIO [56:57]

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Design Notice – GPIO selection (5/8)

- Yellow area is the reset state of “GPIO mode” and “PU/PD” (refer to datasheet chapter 4.4)
- GPIO [41] will be workable after DVDD_NFI (ball T19) active
- GPIO [47:51] will be workable after DVDD_PCM (ball N18) active

- Those UART1 can not used for download !!
- They are just for debugging

- GPIO41 (EINT0) power domain=DVDD_NFI, suggest to reserve for WIFI EINT.

Ball	Name	Default Mode	Mode 0	Mode 1	Mode 2	Mode 3	Default PU/PD	Power domain	Voltage	Schmitt Trigger	Buffer
			Function	Function	Function	Function					strength
External Interrupt Interface											
L24	EINT0	0	GPIO41	EINT0	CLKM4	D2_TID6	PU	DVDD_NFI	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
K24	EINT1	0	GPIO42	EINT1	EDICK	CLKM5	PU	DVDD28	2.8V	Yes	2,4,6,8
L20	EINT2	0	GPIO43	EINT2	EDIWS	UTXD1	PU	DVDD28	2.8V	Yes	2,4,6,8
H24	EINT3	0	GPIO44	EINT3	EDIDAT	URXD1	PU	DVDD28	2.8V	Yes	2,4,6,8
L21	EINT4	0	GPIO52	EINT4	UCTS1	TDMA_D1	PU	DVDD28	2.8V	Yes	2,4,6,8
K23	EINT5	0	GPIO53	EINT5	URTS1	TDMA_CK	PU	DVDD28	2.8V	Yes	2,4,6,8
K21	EINT6	0	GPIO54	EINT6	LPCE1B	TDMA_D0	PU	DVDD28	2.8V	Yes	2,4,6,8
Digital Audio Interface											
N19	DAICLK	0	GPIO47	DAICLK	EDIDAT	MC1CK	PD	DVDD_PCM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
M22	DAIPCMOUT	0	GPIO48	DAIPCMOUT	EDICK	MC1CM0	PD	DVDD_PCM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
M23	DAIPCMIN	0	GPIO49	DAIPCMIN	EDIWS	MC1DA0	PD	DVDD_PCM	1.8V/2.8V	No	2,4,6,8,10,12,14,16
N23	DAIRST	0	GPIO50	DAIRST	LPCE2B	MC1INS	PD	DVDD_PCM	1.8V/2.8V	Yes	2,4,6,8,10,12,14,16
L23	DAISYNC	0	GPIO51	DAISYNC	MC1DA1	NCE1B	PD	DVDD_PCM	1.8V/2.8V	No	2,4,6,8,10,12,14,16

- Generally connect to VIO (ball B5)

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Design Notice – GPIO selection (6/8)

- Yellow area is the reset state of "GPIO mode" and "PU/PD" (refer to datasheet chapter 4.4)
- GPIO [10:13] will be workable after DVDD_MC2 (ball C14) active

Ball	Name	Default Mode	Mode 0 Function	Mode 1 Function	Mode 2 Function	Mode 3 Function	Default PU/PD	Power domain	Voltage	Schmitt Trigger	Buffer strength
PWM Interface											
K18	PWM3	0	GPIO59	PWM3	URXD2	ARM7_JTCK	PD	DVDD28	2.8V	No	4,8,12,16
J18	PWM4	0	GPIO60	PWM4	UTXD2	ARM7_JTDI	PD	DVDD28	2.8V	No	4,8,12,16
J19	PWM5	0	GPIO61	PWM5	URXD3	ARM7_JTMS	PD	DVDD28	2.8V	No	4,8,12,16
K19	PWM6	0	GPIO62	PWM6	UTXD3	ARM7_JTDO	PD	DVDD28	2.8V	No	4,8,12,16
General purpose Input / Output											
J22	GPIO58	0	GPIO58	UTXD1	CLKM4	ARM7_JTRST_B	PU	DVDD28	2.8V	No	4,8,12,16
H19	GPIO63	0	GPIO63	CLKM5	WIFI2BT	ARM7_JRTCK	PD	DVDD28	2.8V	No	4,8,12,16
H22	GPIO64	0	GPIO64	URXD1	BT2WIFI_0	SRCLKENAI	PU	DVDD28	2.8V	Yes	4,8,12,16
Power Management Unit											
C5	SCLK2	1	GPIO66	SCLK2				VSIM2	1.8/3.0V	No	
A2	SIO2	1	GPIO65	SIO2				VSIM2	1.8/3.0V	No	
F9	SRST2	1	GPIO67	SRST2				VSIM2	1.8/3.0V	No	

- GPIO [65:67] will workable after following conditions :

(1) VSIM2 enable
(2) VSIM2_GPIO_EN=1 (refer to VSIM2_CON3 : Vsim2 LDO control register 3)

- Note that the PU/PD is not configurable for GPIO [65:67].
  These pins will automatically pull down when set in GPIO input mode.
  The pull down is disabled when these pins are in GPIO output mode.

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Design Notice – GPIO selection (7/8)

- **Yellow area** is the reset state of “GPIO mode” and “PU/PD” (refer to datasheet chapter 4.4)

Ball	Name	Default Mode	Mode 0 Function	Mode 1 Function	Mode 2 Function	Mode 3 Function	Default PU/PD	Power domain	Voltage	Schmitt Trigger	Buffer strength
USB Interface											
Y1	USB_VRT	0	USB_VRT					AVDD33_USB	3.3V	No	
V3	USB_DP	0	UTXD1	USB_DP				AVDD33_USB	3.3V	No	
U3	USB_DM	0	URXD1	USB_DM				AVDD33_USB	3.3V	No	
MIPI Interface											
AD22	RDN0	0	CMDAT5	RDN0				DVDD28_MIPI	2.8V	Yes	
AD23	RDP0	0	CMDAT4	RDP0				DVDD28_MIPI	2.8V	Yes	
AC23	RCN	0	CMDAT3	RCN				DVDD28_MIPI	2.8V	Yes	
AC24	RCP	0	CMDAT2	RCP				DVDD28_MIPI	2.8V	Yes	
AB24	RDN1	0	CMDAT1	RDN1				DVDD28_MIPI	2.8V	Yes	
AA24	RDP1	0	CMDAT0	RDP1				DVDD28_MIPI	2.8V	Yes	

- USB_DP/DM & UART1 TX/RX share-pad, power domain = AVDD33_USB (3V3)
- In BootROM stage, this share-pad will switch to UART1 TX/RX forFlashTool or META communication. After booting, software will switch share-pad to USB_DP/DM.

- CMDAT[0:5] & MIPI interface (RDP[0:1], RDN[0:1], RCP, RCN) share-pad.
  You can switch this share-pad mode by change CSI2_EN (CSI2_CTRL[8])
- CSI2_EN=0 (default) (refer to CSI2_CTRL[8] : CSI2 control register)

(1) For Parallel mode sensor, don't need to set anything.
(2) For MIPI sensor, please set CSI2_EN=1 (this share-pad will change to mode 1)
  (refer to mcu\custom\drv\image_sensor\MT9P012_MIPI\image_sensor_MT9P012_MIPI.c)

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Design Notice – GPIO selection (8/8)

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Notice of Drv_Tool usage

After enable "InPull En", you can **change the PU/PD value** by changing "InPull SelHigh".
(Only valid when GPIO is **input** mode)

"InPull En" can **enable/disable PU/PD**, then GPIO will be the default PU/PD value after reset state.
(Only valid when GPIO is **input** mode)

"OutHigh" can **change the default output level.**
(Only valid when GPIO is **output** mode)

GPIO Setting | GPO Setting | EINT Setting | ADC Setting | KEYPAD Setting | PMIC Setting

	Def.Mode	M0	M1	M2	M3	InPull En	InPull SelHigh	Def.Dir	In	Out	INV	OutHigh
GPIO0	0:GPIO0	☑	☐			☑ PD	☑	IN	☑	☐	☐	☐
GPIO1	0:GPIO1	☑	☐			☑ PD	☐	IN	☑	☐	☐	☐
GPIO2	0:GPIO2	☑	☐			☐ PD	☐	OUT	☐	☑	☐	☐
GPIO3	0:GPIO3	☑	☐			☐ PD	☐	OUT	☐	☑	☐	☑

In above example :
GPIO0 will be PU in input mode
GPIO1 will be PD in input mode
GPIO2 will be Low in output mode
GPIO3 will be High in output mode

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Design Notice – ADC / TP

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Design Notice – ADC

ADC Channel	Function	Pinout
AUXADC_0	Internal use (VBAT)	N.A. (Internal)
AUXADC_1	Internal use (ISENSE)	N.A. (Internal)
AUXADC_2	Internal use (CHRIN)	N.A. (Internal)
AUXADC_3	Internal use (BATTEMP)	N.A. (Internal)
AUXADC_4	External ADC channel	P3
AUXADC_5	External ADC channel	M4
AUXADC_6	External ADC channel	P2
AUXADC_7	External ADC channel	N4

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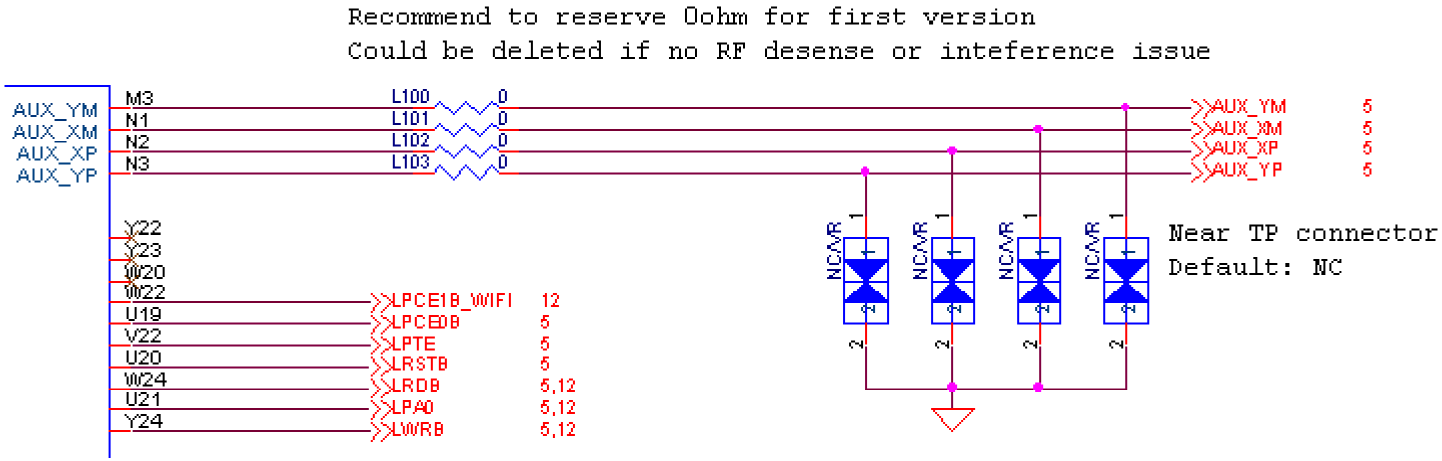
Design Notice – Touch Panel

Confidential B

- Recommend to reserve 0ohm and varistors in the first version.
- For RF desense issue, replace 0ohm with adequate beads.
- For ESD issue, mount adequate varistors.
- Otherwise, these components can be removed in later versions to save BOM cost.



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Design Notice – External Memory Interface

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Design Notice – External Memory Interface (1/2)

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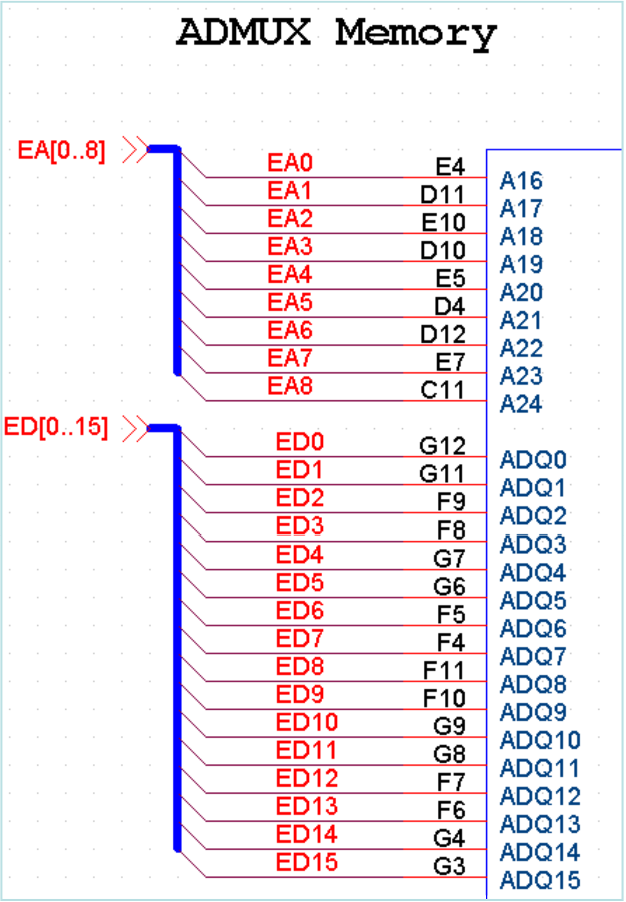
MT6236	External Memory (ADMUX NOR+PSRAM)	External Memory (DDR)	Remark
EA[0:13]	A[16:24]	A[0:13]	Remark 1
EA14 EA15	---	BA0 BA1	
ED[0:15]	ADQ[0:15]	DQ[0:15]	
ECS0_B ECS1_B	NOR_CS# PSRAM_CS#	CS# ---	
ERD_B	OE#	---	
EWR_B	WE#	WE#	
ED_CLK ED_CLK_B	---	CLK CLK#	
EC_CLK EC_CLK_FB	CLK	---	Remark 2 (next page)
ECKE	---	CKE	
EADV_B	ADV#	---	
ECAS_B	---	CAS#	
ERAS_B	---	RAS#	
DQM0	LB#	LDQM	
DQM1	UB#	UDQM	
DQS0	---	LDQS	
DQS1	---	UDQS	
EWAIT	RDY, WAIT	---	
WATCHDOG	RST#	---	
VM	WP#	---	
GND	P_CRE, P_MODE	---	Remark 3 (next page)

Remark 1:
Connect MT6236 EA[0:8] to ADMUX memory higher address bus



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Design Notice – External Memory Interface (2/2)

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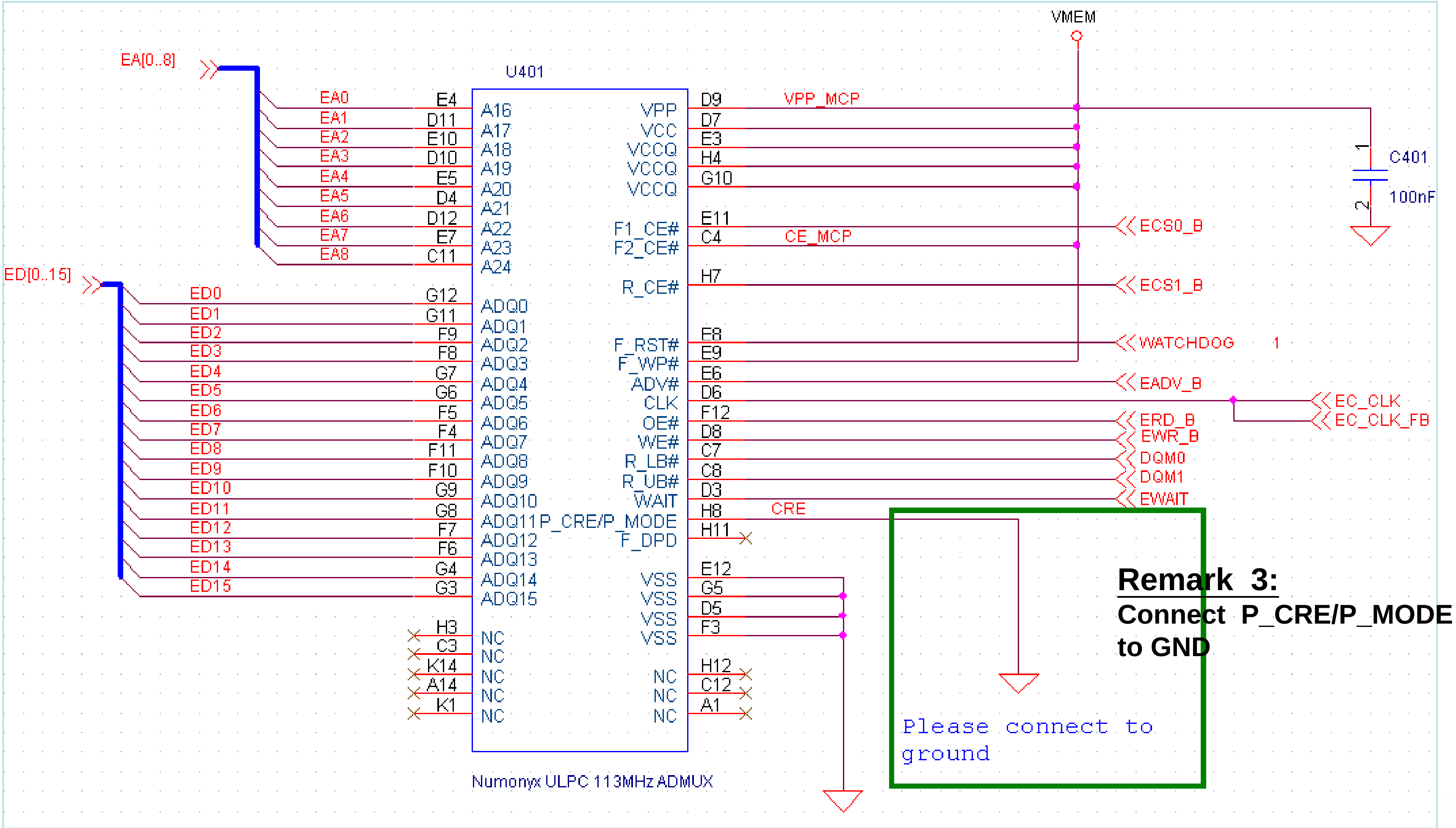
Remark 2:

(1) EC_CLK & EC_CLK_B should be differential trace

(2) The connection of EC_CLK & EC_CLK_FB should be close to memory



Remark 3:

Connect P_CRE/P_MODE to GND

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Design Notice – Camera

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Design Notice – Camera (1/18)

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- **Camera Power Design Notice**

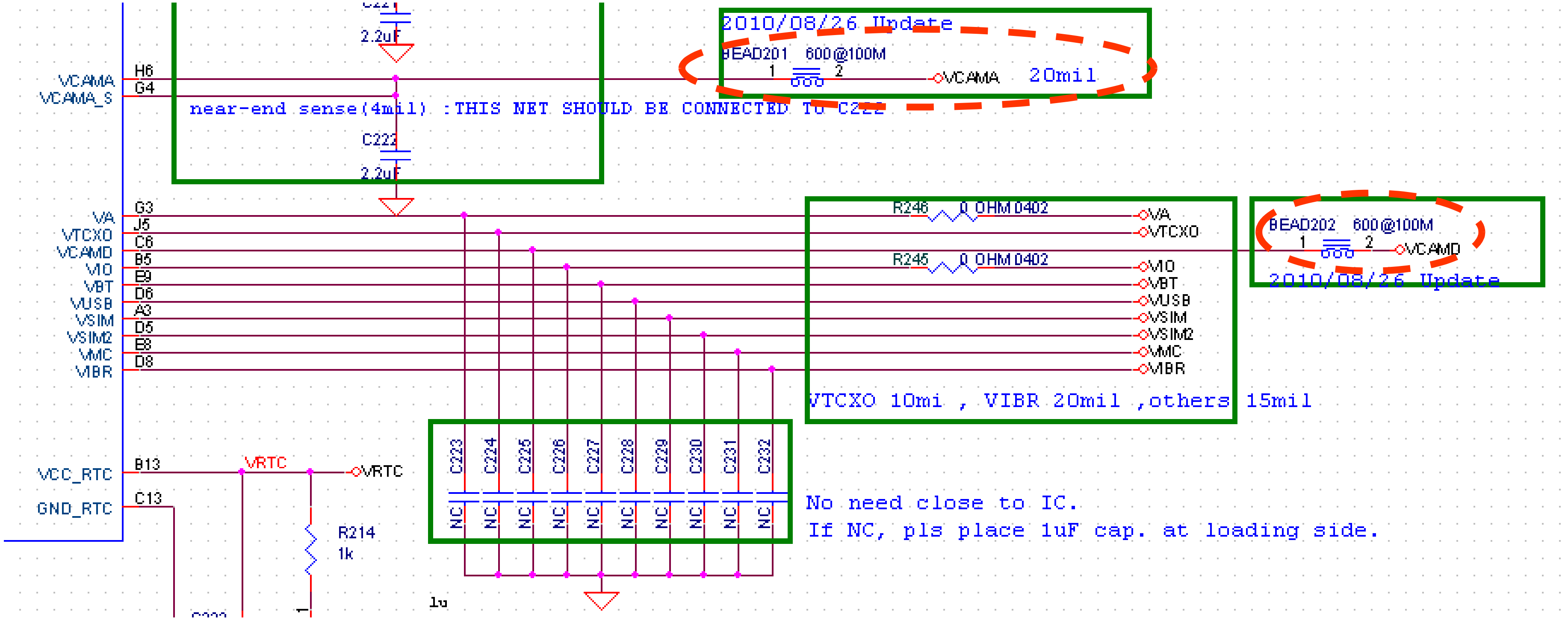
2010/10/12 update camera power design notice :

(1). Config VCAMA=2V8 and connect to DVDD_CAM (pin Y19) and Camera DOVDD and Camera AF power

(2). Config VCAMD=1V5 and connect to Camera DVDD

(3). Add external LDO (250mA, PSRR=VCAMA) for Camera AVDD

(4). Add bead (600@100M) on above three camera power source



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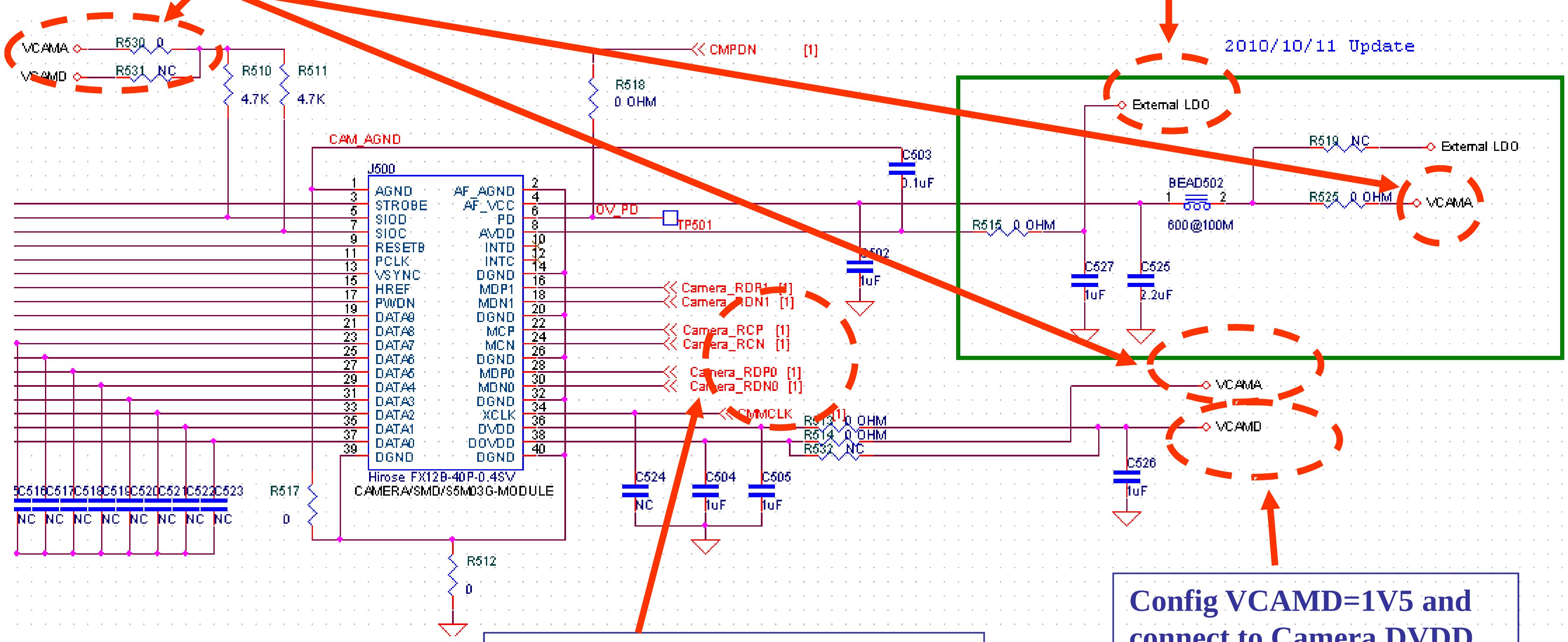
Design Notice – Camera (2/18)

- **Camera Reference Circuit (1/4):**

Config VCAMA=2V8 and connect to DVDD_CAM (pin Y19) ,Camera DOVDD and Camera AF power

Add external LDO (250mA, PSRR=VCAMA) for Camera AVDD



For MIPI sensor,

EMI filter cap. max. loading is 3pf

Config VCAMD=1V5 and connect to Camera DVDD

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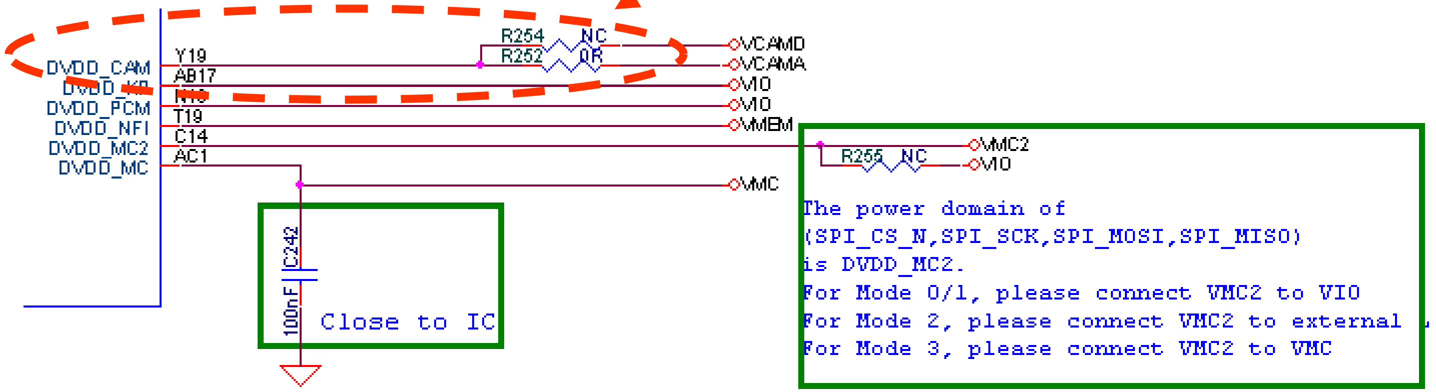
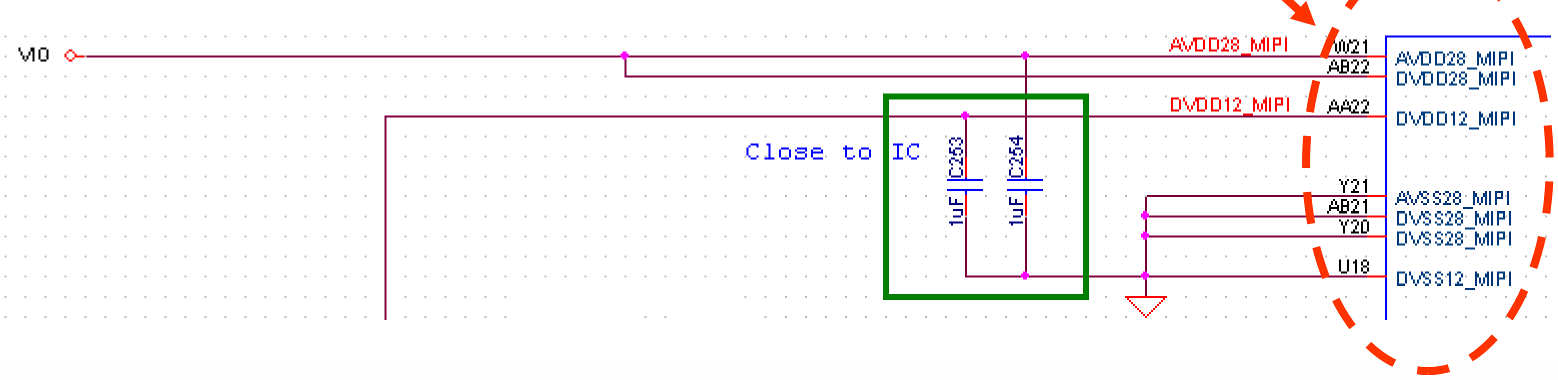
Design Notice – Camera (3/18)

- **Camera Reference Circuit (2/4):**

Config VCAMA=2V8 and connect to DVDD_CAM (pin Y19) ,Camera DOVDD and Camera AF power



MIPI Camera interface power



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Design Notice – Camera (4/18)

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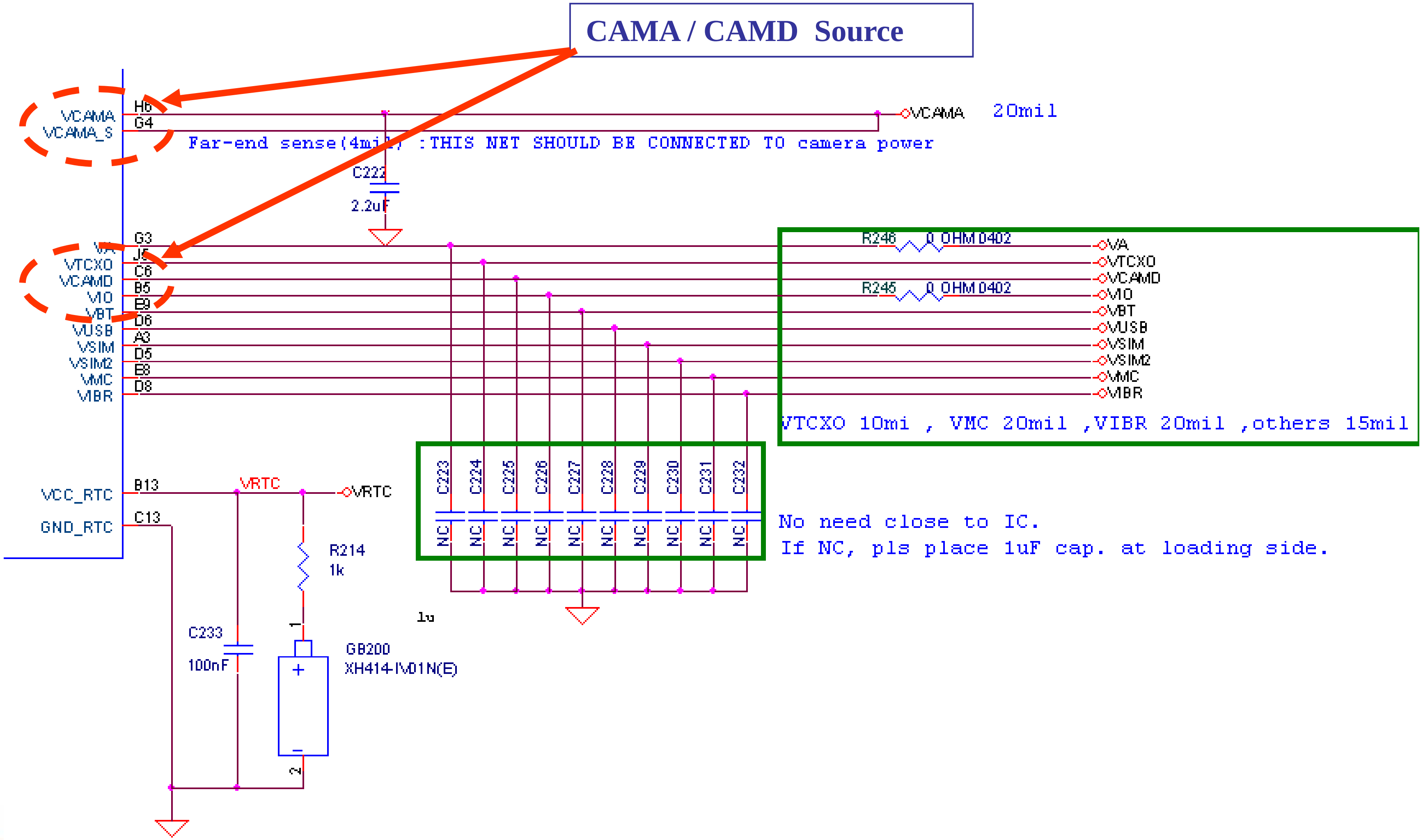
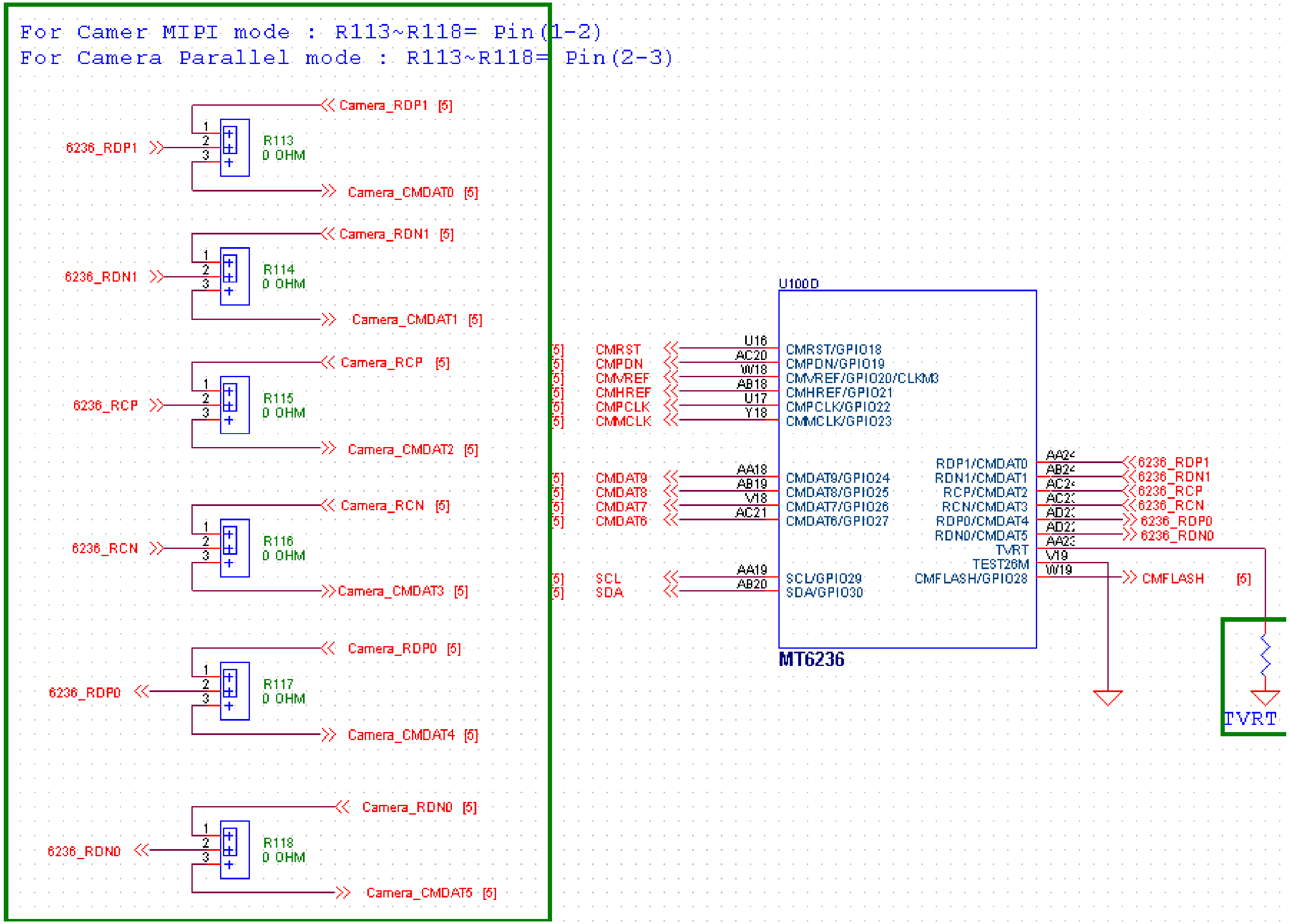
- **Camera Reference Circuit (3/4):**



Design Notice – Camera (5/18)

Confidential B

- **Camera Reference Circuit (4/4):**



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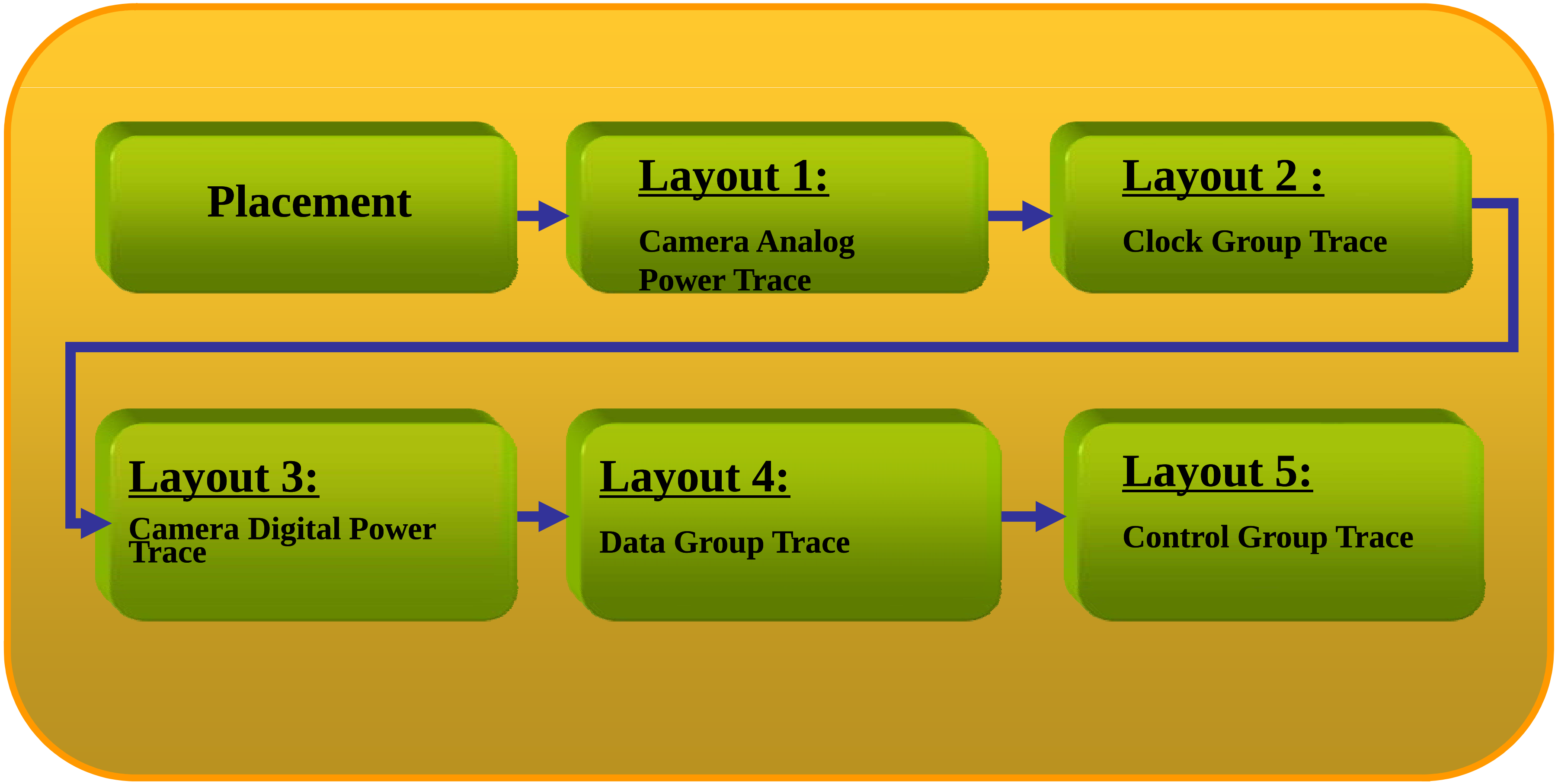
Design Notice – Camera (6/18)

- **PCB Design Flow :**



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Design Notice – Camera (7/18)

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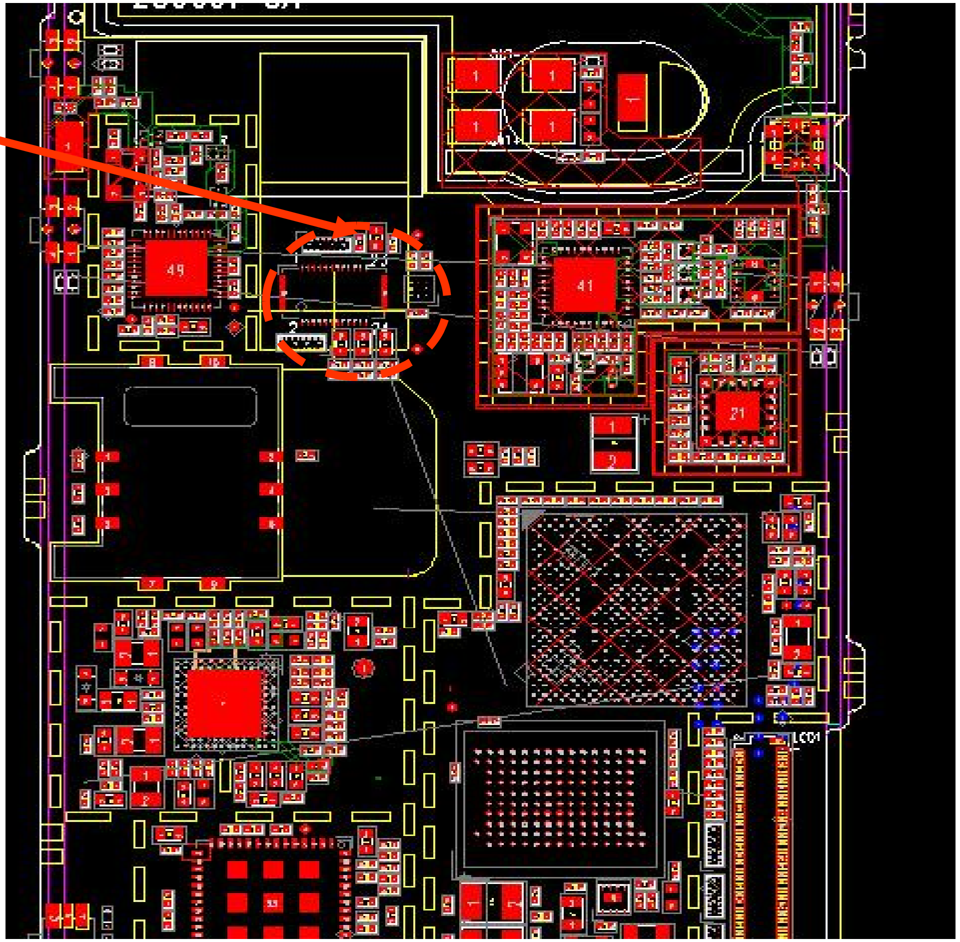
- **PCB Component Placement :**

➢To minimize RF radiation interference, do not place the sensor module near or beneath the antenna.

➢The sensor module’s power supplies(inductors , beads , resistors , capacitors) should be placed as close as possible to the connect



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Design Notice – Camera (8/18)

- **Single Camera - Image Sensor Interface :**

The Image Sensor interface is divided up into three groups summarized in below that each group has special routing guidelines. The interconnecting lengths in the controller package should be calculated for the length matching.

Group	Signal Name	Description
Data	DQ[0:9] CMVREF CMHREF	Image sensor data[0:9] input Image sensor vertical reference signal input Image sensor horizontal reference signal input
Clock	MCLK PCLK	Image sensor master clock output Image sensor pixel clock input
Control	SCL SDA CMRST CMPDN	I2C clock output I2C data input/output Image sensor reset signal output Image sensor power down signal output

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Design Notice – Camera (9/18)

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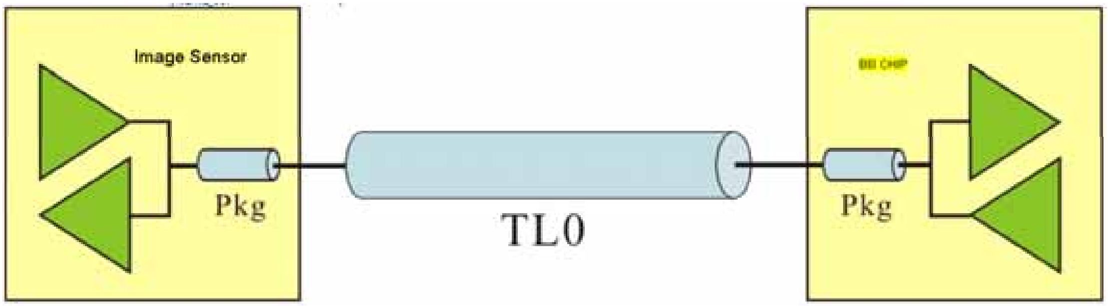
Single Camera - PCB Layout Design Notice (1/4)

This section states the layout recommendations for the Image Sensor data group routing. Refer to below figure for the data group topology and below table for the routing guidelines. Suggest data group should avoid clock or noisy power in upper/lower layer



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Image Sensor Data)	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 (BB ball to Image Sensor Connect)	4,800 mils
Length matching	Max. (Trace length) − 500mil ≤ (Trace length) ≤ Max. (Trace length)
Remark	Suggest data group should avoid clock or noisy power in upper/lower layer

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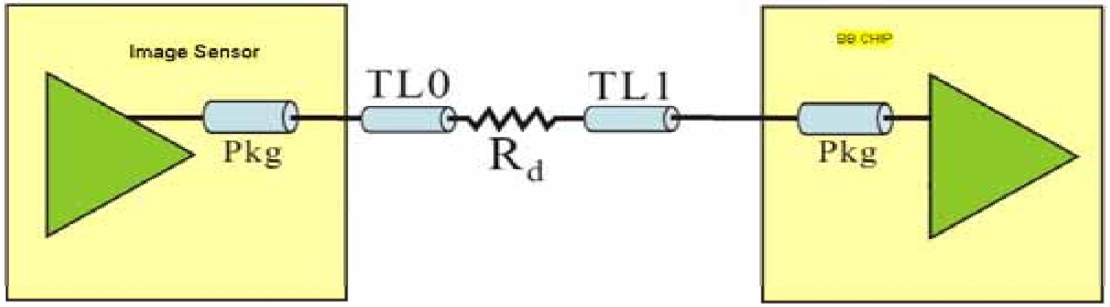
Design Notice – Camera (10/18)

Confidential B

- ## Single Camera - PCB Layout Design Notice (2/4)

This section states the layout recommendations for the Image Sensor clock signals. Refer to below figure for the clock topology and below table for the routing guidelines. Each clock shall be routed surround with ground plan. The R_d is optional that could be different from 0 or 22 Ω if the different controller I/O is designed or the different driving strength is assigned.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground plane.
Main trace patterns (MCLK PCLK)	W = 4-mil, S ≥ 4-mil.Surround the CLK with ground plan.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Damping resistor (R_d)	Optional, 0 or 22 Ω (Near the Image Sensor).
Max. (TL0 + TL1)	4,500 mils
Length matching for Data-to-PCLK	(PCLK length − 500-mil) ≤ DQ length ≤ (PCLK length + 500-mil)
Remark	Each clock shall be routed surround with ground plan

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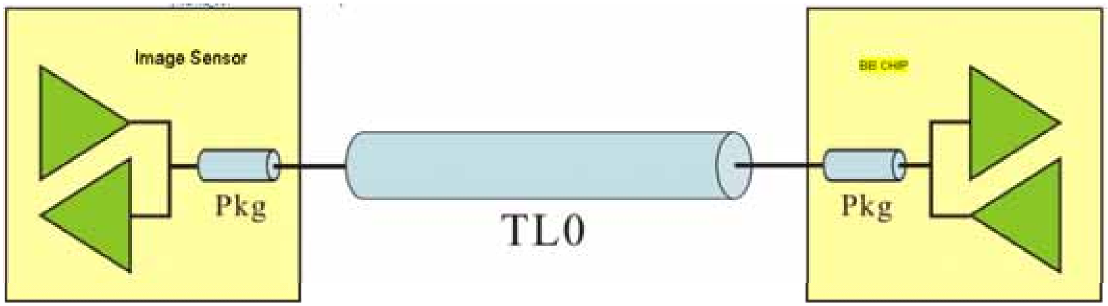
Design Notice – Camera (11/18)

Single Camera - PCB Layout Design Notice (3/4)

This section states the layout recommendations for the Image Sensor control signals. Refer to below figure for the control topology and below table for the routing guidelines.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0	6000 mils
Remark	Suggest control group should avoid clock or noisy power in upper/lower layer

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Design Notice – Camera (12/18)

Single Camera - PCB Layout Design Notice (4/4)

This section states the layout recommendations for the MIPI CSI signals. Refer to below tables for the routing guidelines. Multiple vias shall be drilled in the ground guard to minimize the inductance of grounding path.

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
PP material	1080
Main trace patterns and impedance (MIPI-CSI)	Target impedance: $Z_{diff} = 100\ \Omega \pm 15\%$. W = 4-mil, S = 7-mil, and Ground Space = 10-mil (GSSG pattern, 20-mil ground guard width).
Maximum length	MIPI CSI: 3 inches.
Length matching in PCB	Pair to pair (within one connector): 100 mils.
Remark	Route the differential pair straight and symmetrically on the same layer with equal trace width and space.

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Design Notice – Camera (13/18)

Confidential B

- **Dual Camera - Image Sensor Interface :**

The Image Sensor interface is divided up into three groups summarized in below that each group has special routing guidelines. The interconnecting lengths in the controller package should be calculated for the length matching.

Group	Signal Name	Description
Data	DQ[0:9] CMVREF CMHREF	Image sensor data[0:9] input Image sensor vertical reference signal input Image sensor horizontal reference signal input
Clock	MCLK PCLK	Image sensor master clock output Image sensor pixel clock input
Control	SCL SDA CMRST CMPDN CMFLASH	I2C clock output I2C data input/output Image sensor reset signal output Image sensor power down signal output Image sensor Flash signal output

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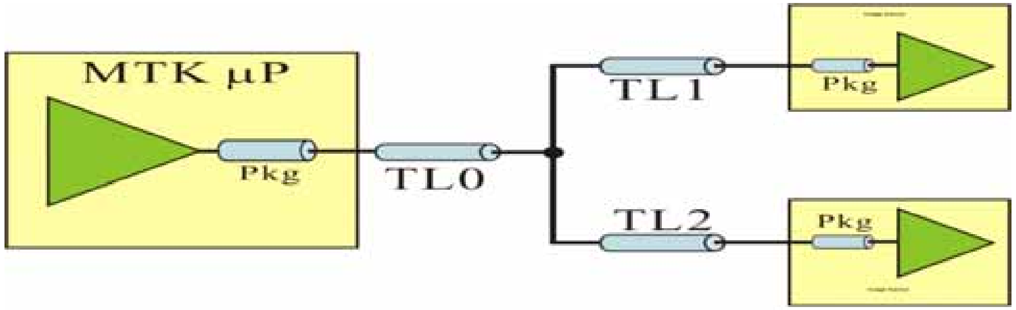
Design Notice – Camera (14/18)

Confidential B

- **Dual Camera - PCB Layout Design Notice (1/3)**

This section states the layout recommendations for the dual camera image sensor data group routing. Refer to below figure for the data group topology and below table for the routing guidelines. Data group shall be routed surround with ground plan



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Image Sensor Data)	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 + TL1 (BB ball to Main Image Sensor Connect)	4,800 mils
Max. TL1 (Branch points to Sub Image Sensor Connect)	1,500 mils
Length matching(TL0+TL1)	Max. (Trace length) − 500mil ≤ (Trace length) ≤ Max. (Trace length)
Remark	Suggest data group should avoid clock or noisy power in upper/lower layer

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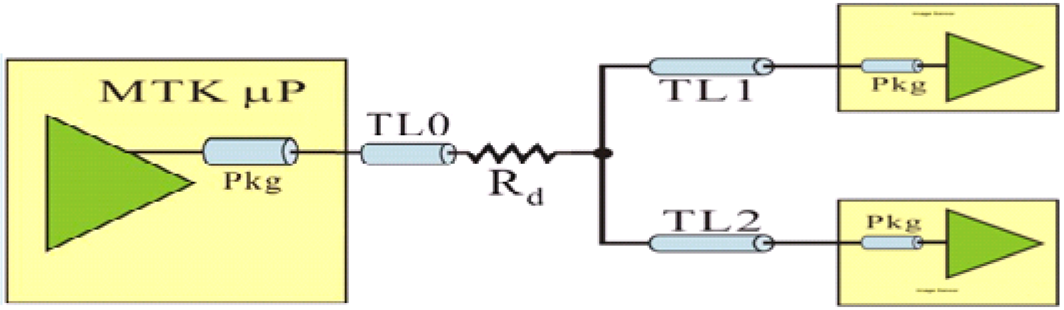
Design Notice – Camera (15/18)

- **Dual Camera - PCB Layout Design Notice (2/3)**

This section states the layout recommendations for the Image Sensor clock signals. Refer to below figure for the clock topology and below table for the routing guidelines. Each clock shall be routed surround with ground plan. The R_d is optional that could be different from 0 or 22 Ω if the different controller I/O is designed or the different driving strength is assigned.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground plane.
Main trace patterns (MCLK PCLK)	W = 4-mil, S ≥ 4-mil.Surround the CLK with ground plan.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Damping resistor (R_d)	Optional, 0 or 22 Ω (Near the Image Sensor).
Max. TL0 + TL1 (BB ball to Main Image Sensor Connect)	4,500 mils
Max. TL1 (Branch points to Sub Image Sensor Connect)	1,500 mils
Length matching for Data-to-PCLK(TL0+TL1)	(PCLK length − 500-mil) ≤ DQ length ≤ (PCLK length + 500-mil)
Remark	Each clock shall be routed surround with ground plan

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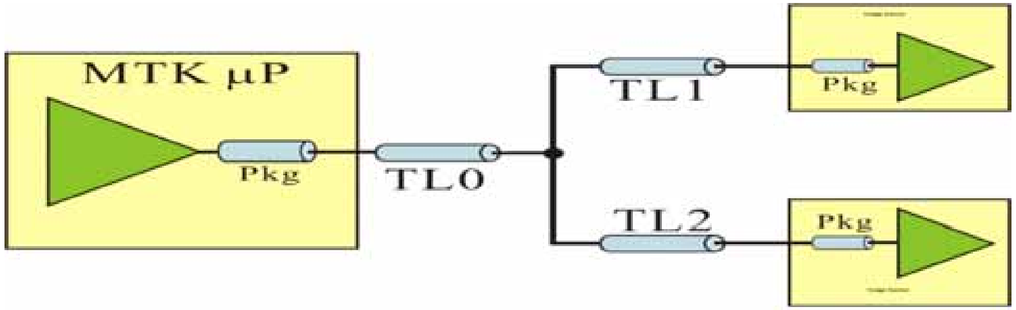
Design Notice – Camera (16/18)

- **Dual Camera - PCB Layout Design Notice (3/3)**

This section states the layout recommendations for the dual Image Sensor control signals. Refer to below figure for the control topology and below table for the routing guidelines.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 + TL1 (BB ball to Main Image Sensor Connect)	6,000 mils
Max. TL1 (Branch points to Sub Image Sensor Connect)	2,000 mils
Remark	Suggest control group should avoid clock or noisy power in upper/lower layer

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Design Notice – Camera (17/18)

● Analog Power Routing

This section states the layout recommendations for the image sensor Analog power routing. Refer to below table for the routing guidelines. Analog Power shall be routed surround with ground plan

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Analog Power)	W ≥ 12-mil, S = 4-mil with GND trace.
Remark	Analog power shall be routed surround with ground plan

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Design Notice – Camera (18/18)

Confidential B

Digital Power Routing

This section states the layout recommendations for the image sensor digital power routing. Refer to below table for the routing guidelines. Digital Power shall be routed surround with ground plan

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Digital Power)	W ≥ 12-mil, S = 4-mil with GND trace.
Remark	Digital power shall be routed surround with ground plan

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Confidential B

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Design Notice – De-sense

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Design Notice – FM de-sense (1/2)

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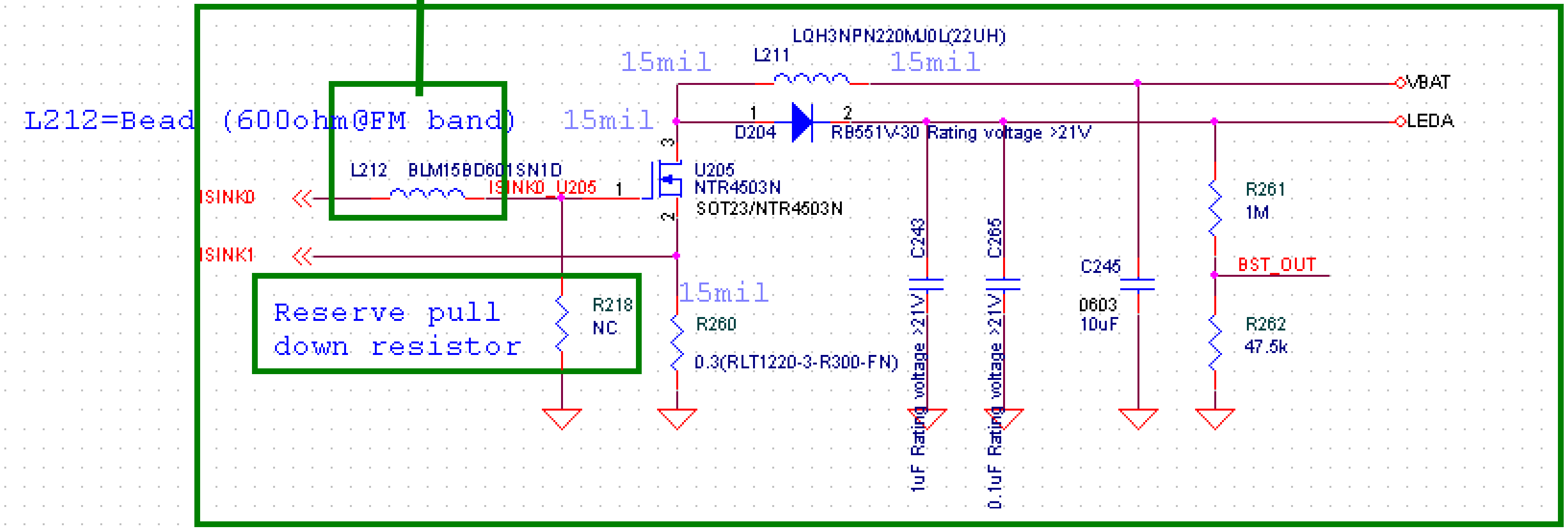
- **LCM backlight causes 1MHz de-sense**

Adding a 600ohm bead here can remove 1MHz-spacing de-sense

Period =1MHz



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Design Notice – FM de-sense (2/2)

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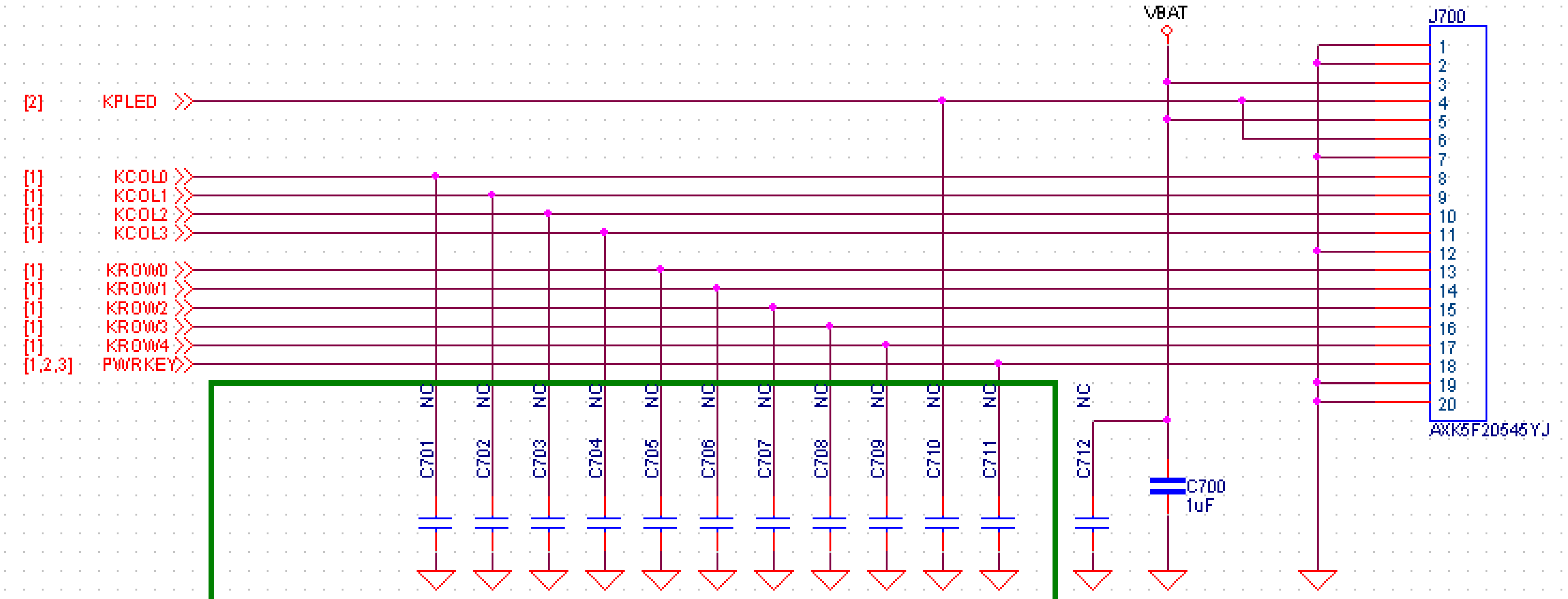
- **Keypad connector is a de-sense path**



Keypad trace could couple noise and cause FM band de-sense, so keypad trace please keep away from clock trace.

If you cannot follow above rule, please reserve 1nf bypass cap in all keypad connector pins.

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FM De-Sense Layout Guide (1/3)

- Earphone jack plays a role as FM antenna port and can't be located near any noisy source including LCM FPC, un-shielding memory/LCM/USB bus, un-shielding boost/charge pump/class D amplifier/bulk/backlight driver circuit, un-shielding PWM signal, etc.
- FMANT trace between earphone jack and FM chip must be enclosed well with GND shielding
  - If FMANT routs in inner layer, not only left and right GND shielding but also up and down GND shielding are necessary for FMANT
  - To keep shorter FMANT trace between earphone jack and FM chip is appreciated if possible
  - GND shielding has to accompany with enough GND vias
- FM_32k trace must be enclosed well with GND shielding

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FM De-Sense Layout Guide (2/3)

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- Noisy sources or traces must be put in shielding cover or shield well with PCB GND layer
  - Noisy source includes LCM FPC, memory/LCM/USB bus, boost/charge pump/class D amplifier/bulk/backlight driver circuit, PWM signal, etc.
- Reserve FM band series bead or EMI filter for possible couple path
  - Series bead(BLM18BD252SN1) close to earphone jack for each audio trace (Audio-L, Audio-R, MIC)
  - Series bead for PMU internal boost input VBAT path ; Series bead for external boost PWM signal path. Bead is put close to radiation source
  - Reserve series 0ohm for parallel host I/F control signal path such as LWRB (write strobe signal) and LPA0(address output)
  - Reserve 2012 size 4 channel EMI filter array (LC type) for LCM data bus and close to LCM connector if necessary

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FM De-Sense Layout Guide (3/3)

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- Put FM chip away from noisy traces or sources and keep L2 GND layer under FM chip as complete as possible
- Others
  - In order to suppress LCM radiation, proper PCB exposed GND area(1/4 LCM metal area at least is recommended) reserving for LCM metal solid grounding is recommended
  - Keep LCM FPC as short as possible; Well GND shielding FPC is appreciated
  - VCO inductor of FM chip has to well GND shielding

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Design Notice – Others (Tool Version)

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Tool version that supports MT6236 development

Tool	Support version
ATE Tool (including SN WRT Tool)	After 10.28
META Tool (including META_DLL)	After v6.1028.0
META_APP_DLL Tool	After v6.1028.0
MultiportDownload Tool	After v3.1028.00
FlashTool	After FlashTool v3.1028.00

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Layout Notice

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Priority for Layout Placement / Routing

Please follow layout priority to process placement/routing.

Layout priority	Function	Risk of "not follow layout rule"
1	High speed memory LPDDR	EMI timing margin not enough ex : (1)Power on fail/unstable (2)System unstable in NT/HT/LT
2	2G/3G I/Q interface, RF interface, SYSCLK	System unstable & Performance risk ex: (1)SYSCLK unstable (2)RF related performance
3	High speed peripheral ex: USB 2.0 high speed, MIPI, SATA,HDMI	Performance risk ex: USB throughput, noise issue
4	Analog audio interface / speech / Class B/D	Performance risk ex: TDD noise, speech/audio noise
5	FM	Performance risk ex: FM related performance
6	RTC	Performance risk (1) 32k timing unstable (2) 32k related function unstable
7	PMU interface ex: Switching regulators, charger, VBAT input, LDOs, Backlight, CamA	System unstable & Performance risk ex: (1) Power supply/sink unstable (2) Analog function performance issue (3) Noise interference issue
8	LCM / Camera / ATV	Performance risk ex: noise issue
9	Memory card, SDIO	Performance risk ex: throughput issue
10	SIM, touch panel	Performance risk
11	UART, SPI, I2C, I2S, PCM	Performance risk
12	JTAG, debug, test mode, GPIOs, key matrix, reset	Performance risk

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Layout Notice (1/5)

0. PCB layer : MT6236 support 6 layer PCB layout.

1. Power trace :

(1) VCORE, VM, VRF, VIBR, VCAMA : 20mil at least

(2) VMC, VA, VCAMD, VIO, VBT, VUSB, VSIM, VSIM2 : 15mil at least

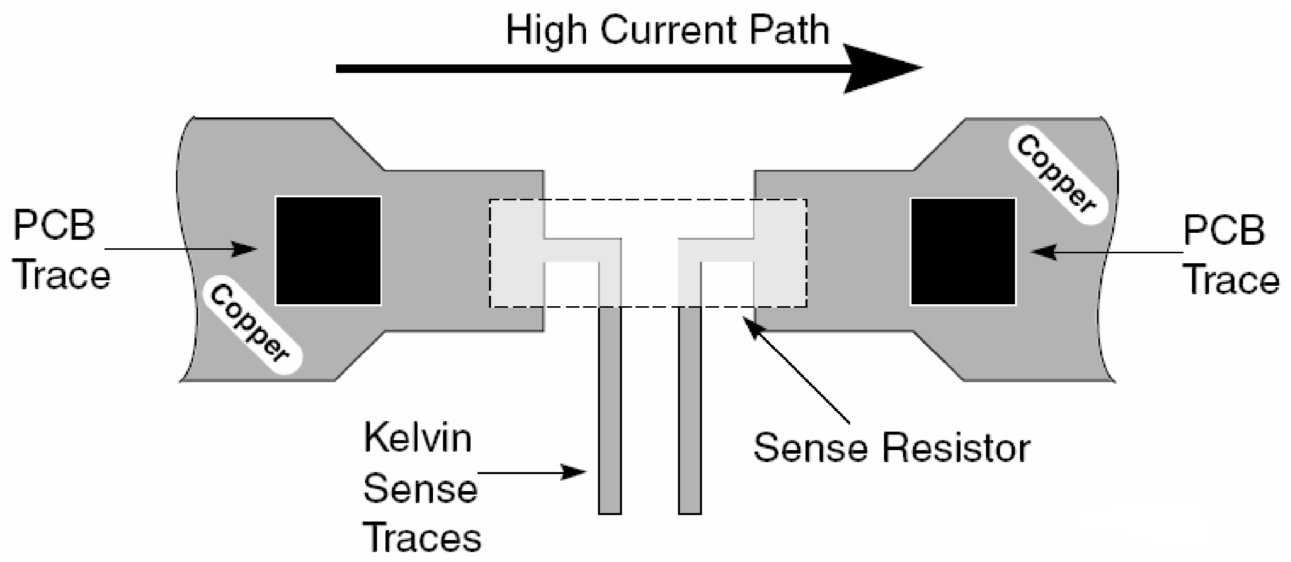
(3) VTCXO : 10mil at least

(4) Charging path : VCHG~VBAT: 40mil at least

(5) Connect Rsense to BATSNS(D3 pin) directly [Please refer to following diagram]

Connect Rsense to ISENSE(C5 pin) directly [Please refer to following diagram]

4mil differential line between ISENSE and BATSNS



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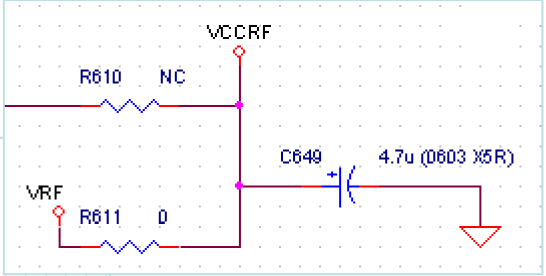
Layout Notice (2/5)

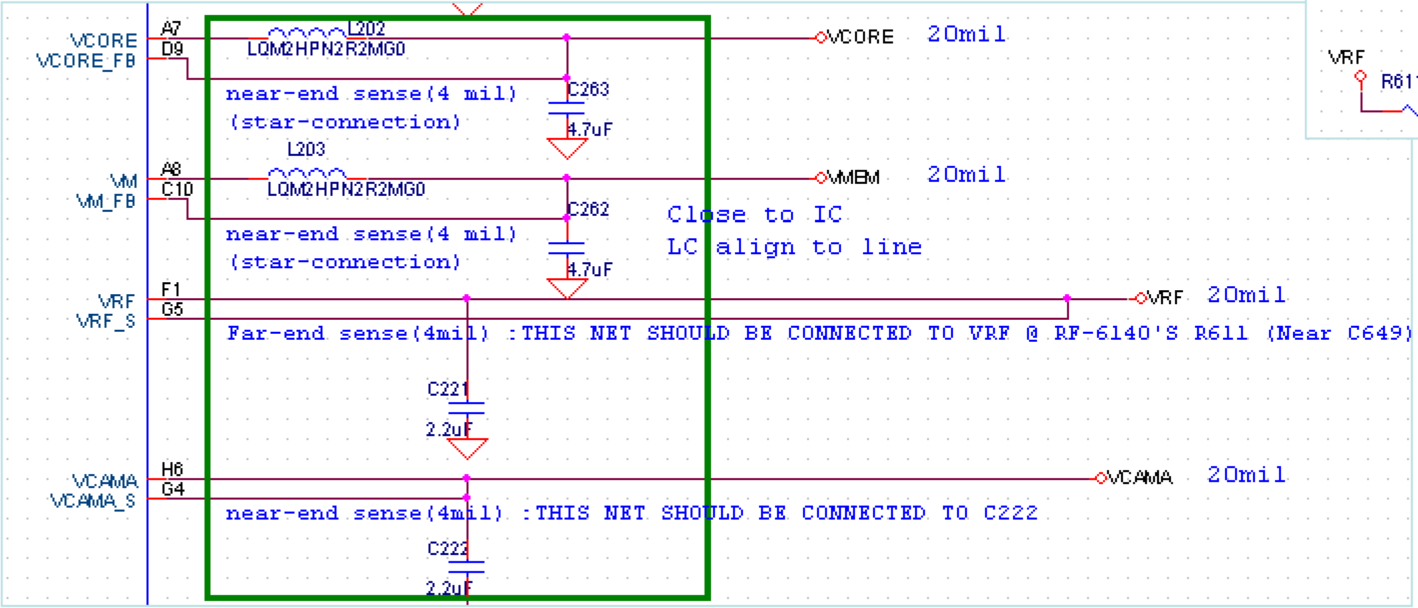
1. Power trace :

(6) For buck mode of VCORE/VM please layout the shortest layout trace from BB output to inductance to bypass capacitor.

(7) For VRF_S : far-end sense trace, please connect it to 6140'S R611 (Near C649)

(8) For VCAMA_S : near-end sense trace, please connect it to C222





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Layout Notice (3/5)

2. Audio trace : (Common rule [1]Protect following traces by GND on upper layer, lower layer, left side, and right side [2]Avoid the crossover with power traces)

(1) AU_VIN0_P/N, AU_VIN1_P/N, AU_OUT0_P/N : Differential line ; the same trace length

(2) AU_MOUT/AU_MOUTL : The same trace length

(3) AU_FMINR/AU_FMINL : The same trace length ; Use GND to separate AU_FMINR and AU_FMINL

(4) AU_MICBIAS_P

3. RF related trace : (Common rule [1]Protect following traces by GND on upper layer, lower layer, left side, and right side [2]Avoid the crossover with power traces)

(1) BDLAIP/BDLAIN, BDLAQP/BDLAQN : Differential line ; the same trace length

(2) APC, AFC

(3) SYSCLK(26MHz)

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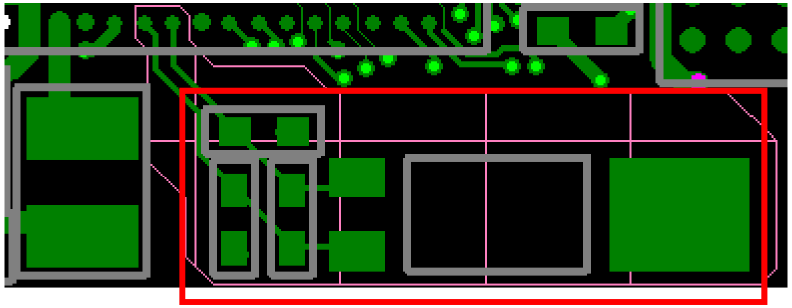
Layout Notice (4/5)

4. Clock related trace : (Common rule [1]Protect following traces by GND on upper layer, lower layer, left side, and right side [2]Avoid the crossover with power traces)

(1) 32kHz :The shortest path ;Please keep the layer clearance in upper and lower layer related to 32kHz traces ;Keep Xout and Xin trace away from buck Vcore/VM (Notice: they are close in the IC ball map:Xin-A13,Xout-A14)



(2) EC_CLK , EC_CLK_FB, ED_CLK, ED_CLK_B

(3) CMMCLK, CMPCLK, DAICLK, SIMCLK : No need to protect those traces by GND, but please keep 8mil distance with other traces

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Layout Notice (5/5)

5. USB related trace : Due to USB2.0 SCH/Layout are both critical, please refer to "MTK_USB_Application_Notes" to get more information

6. Reset related trace : (Common rule [1]Please keep 8mil distance with other traces [2]Please keep 50mil distance with shielding case and PCB edge.

(1) RESETB , SYSRST_B

(2) WATCHDOG

(3) LRSTB

(4) SIMRST

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Issue Case Study

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Issue Case Study - 1

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Issue date : 2010/08/26

[Issue description]

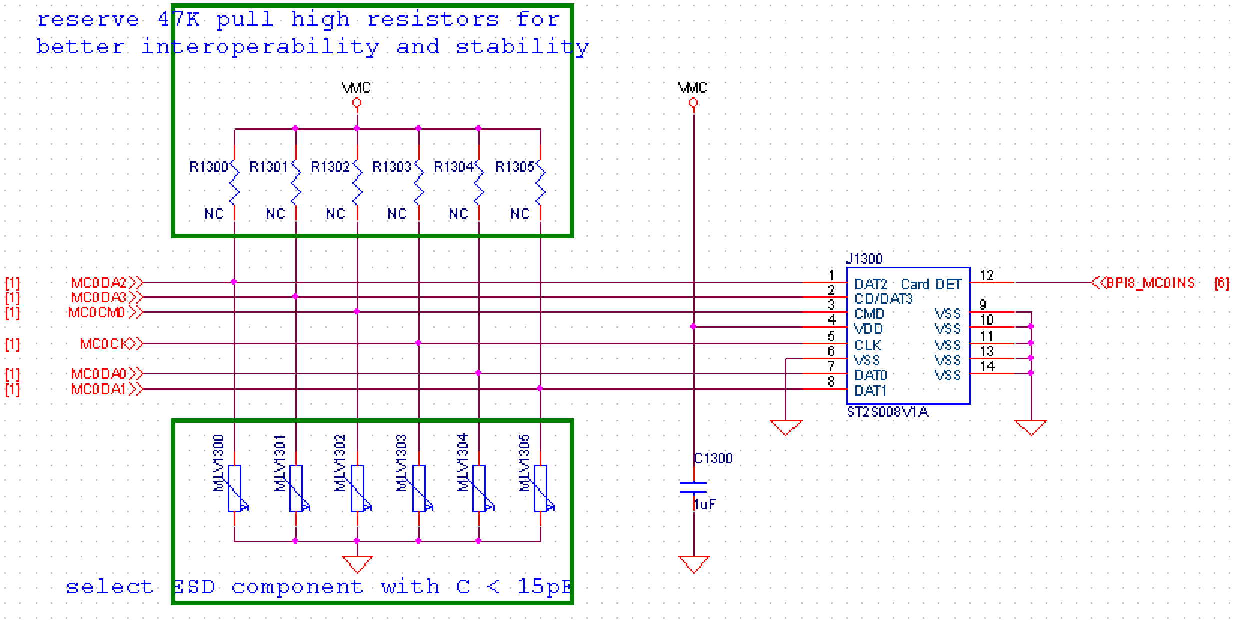
MSDC IOT issue : MT6236 cannot detect MSDC after some bad quality MSDC card plug-in

[Root cause]

1. SD2.0 spec define "MSDC controller + PCB trace + card" total capacitor loading < 40pF. Normally card internal capacitor loading<10pf, so old ref. design suggest to adopt ESD component with C<30pf.
But some bad quality MSDC card has larger capacitor loading (>10pf) and cause IOT issue.
2. SD2.0 spec define VMC=2V7~3V6, MT6236 set VMC=2V8 default

[Solution]

1. For better MSDC IOT, customer can choose ESD component with smaller C (<15pf)
2. For better MSDC IOT, customer can configure VMC=3V3 default.



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Issue Case Study - 2

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Issue date : 2010/09/30

[Issue description]

EINT 7 is MUX with URXD1 ; EINT8 is MUX with URXD2; EINT9 is MUX with URXD3
EINT10 is MUX with IRDA_RX

Remember EINT7~10 is valid in order, for example of EINT 8 (URXD2) :
EINT 8 (URXD2) MUX in three pins (1)GPIO31 (2)GPIO45 (3)GPIO59,
And the order is GPIO31 > GPIO45 > GPIO59, it means
If GPIO31=mode 2, URXD2=GPIO31
else if GPIO45=mode 1, URXD2=GPIO45
else if GPIO59=mode 2, URXD2=GPIO59
Else URXD2=1

And even if EINT 8 (URXD2) MUX in three pins, you can only choose 1 pin to be EINT 8 (URXD2) at the same time !

Ball	Name	Default Mode	Mode 0 Function	Mode 1 Function	Mode 2 Function	Mode 3 Function
U3	USB_DM	0	URXD1	USB_DM		
H24	EINT3	0	GPIO44	EINT3	EDIDAT	URXD1
H22	GPIO64	0	GPIO64	URXD1	BT2WIFI_0	SRCLKENAI
Y22	LSA0	0	GPIO31	LSA0	URXD2	CLKM3
M18	URXD2	0	GPIO45	URXD2	UCTS3	D2_TID2
K18	PWM3	0	GPIO59	PWM3	URXD2	ARM7_JTCK
AA16	KROW7	0	GPIO16	KROW7	EDIDAT	URXD3
M19	URXD3	0	GPIO39	URXD3	UCTS2	D2_TID4
J19	PWM5	0	GPIO61	PWM5	URXD3	ARM7_JTMS
K20	IRDA_RXD	3	GPIO56	IRDA_RXD	PWM4	UCTS1

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Appendix : MT6236 High Speed Memory Layout Rule(DDR)

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High Speed Memory Layout

- Memory PCB layout characteristics in the following order:
  1. Placement
  2. Ground/Power plane
  3. Suggested routing order (Signal layout)
  4. Other general layout considerations

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DDR SDRAM signals

- We can categorize DDR SDRAM interfaces into 4 groups as follows.

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask
Clock	CLK CLK#	Memory Differential Clock Memory Inverted Differential Clock
Command	A[0:15] BA[0:1] RAS CAS WE	Address Bus Bank Select Row Address Select Column Address Select Write Enable
Control	CKE CS	Clock Enable Chip Select

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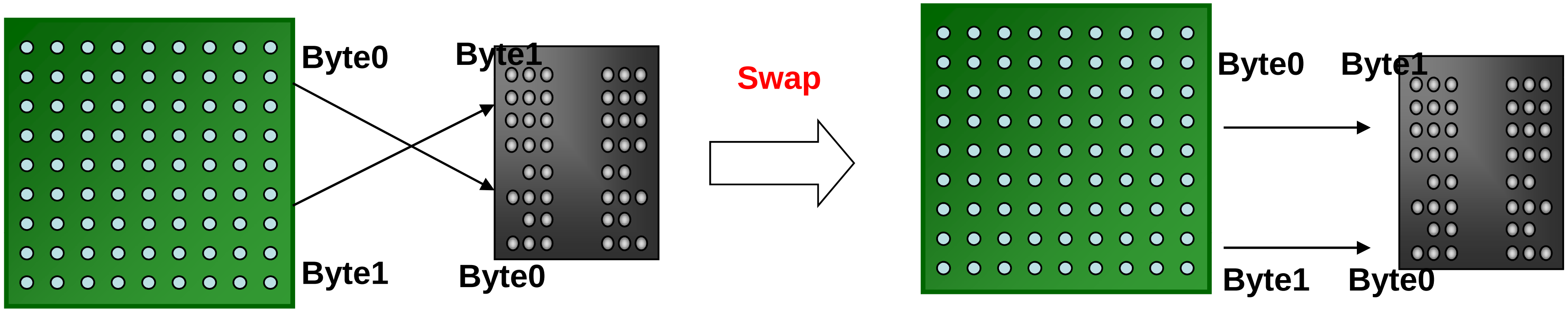
High Speed Memory Layout

- Placement
  - Memory device must place as close to BB Chip as possible
  - Avoiding extra long trace (Max trace1500mil)
  - Avoiding other high frequency devices place close to Memory
  - Route these traces smoothly, reduce the via counts and avoiding traces interlace if possible
  - You can swap byte in order to reduce traces interlace if there has restriction in placement



  - "Swap byte" means to connect DQS0 from BB chip to memory DQS1 in order to reduce the interlacing of data traces, e.g. DQ[0:7] from BB chip to memory D[8:15].

    Note: Swap the corresponding DQSx ,DMx and DQx at the same time.
  - Different bits (DQx) in the same data byte could also be swapped if needed.

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High Speed Memory Layout

- Ground/Power plane
  - A solid power/ground plane must be provided near all traces routing layers.
  - It will minimize the return current path to get better performance.
  - There are 2 methods for reference:
    1. It is recommended all traces are routed above a solid GND plane, and there is a power plane (memory power domain VMEM) under the GND plane if possible.

e.g. 6 layers(MT6236 reference stack up)-

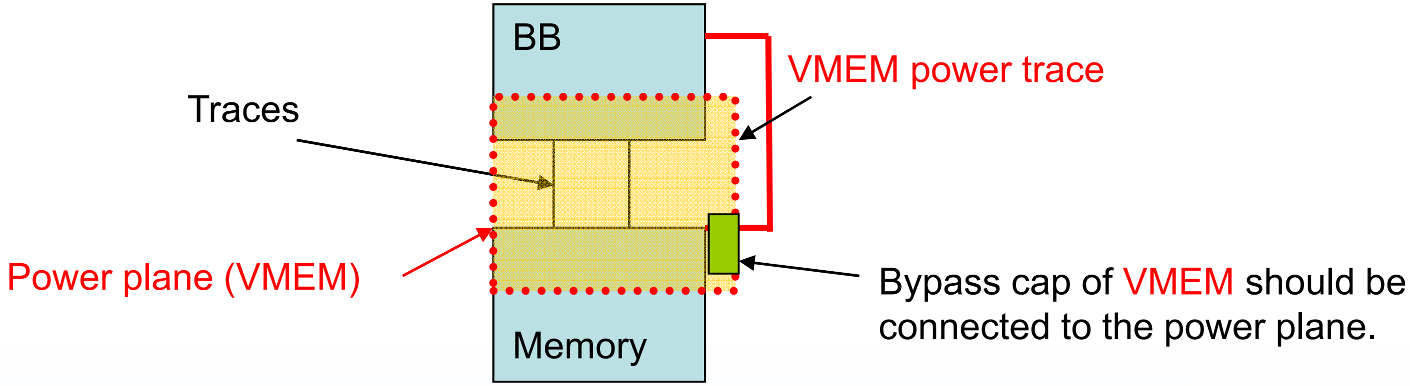
1st layer : memory traces

2nd layer: memory traces (strongly recommended - the same group of traces routed on the same layer)

3rd layer: GND

4th layer: Power plane (VMEM), it could including some memory traces (need to shielded with Vm plane)

5th/6th layer: if there is some memory trace in 4th layer, please assign 5th layer as GND plane. If there is no memory trace in 4th layer, 5th/6th don't care.



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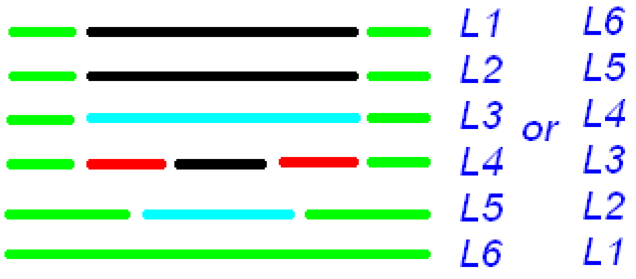
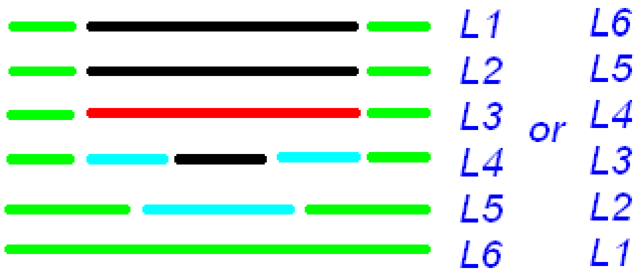
High Speed Memory Layout

2. If power plane is a signals' reference plane (return current path), please notice that its area must be cover the entire signal routes in signal layer. In this condition, GND plane is still needed even as 6th layer

Method 1:



Method 2:



Black line: Memory Signal traces Blue line: GND plane Red line: Power plane

Green line: do not care

Note: All power trace bypass capacitors (de-cap) must be placed as close to the memory or BB power pins as possible, and all capacitor's GND should have the shortest and widest trace to the GND plane.

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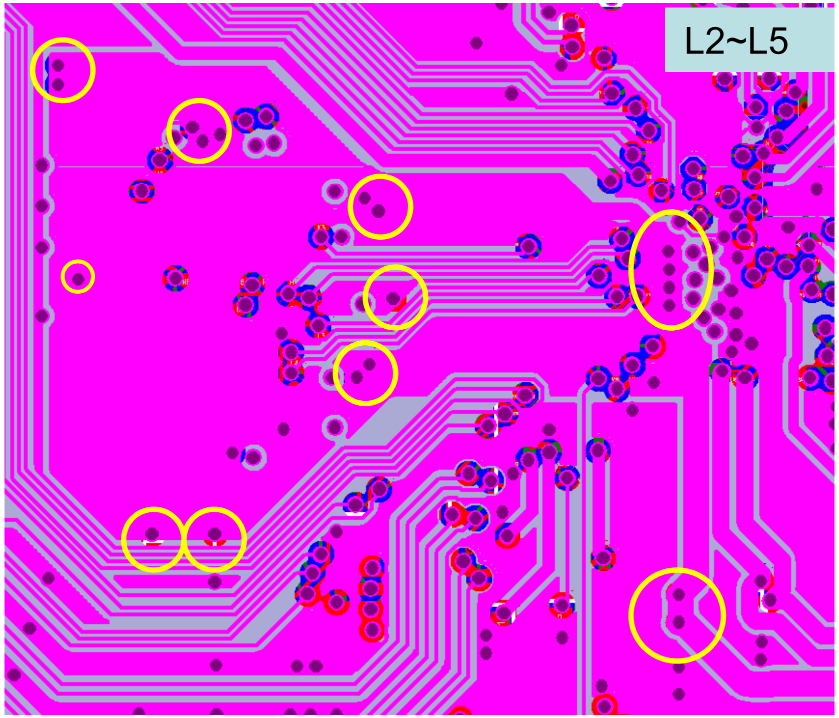
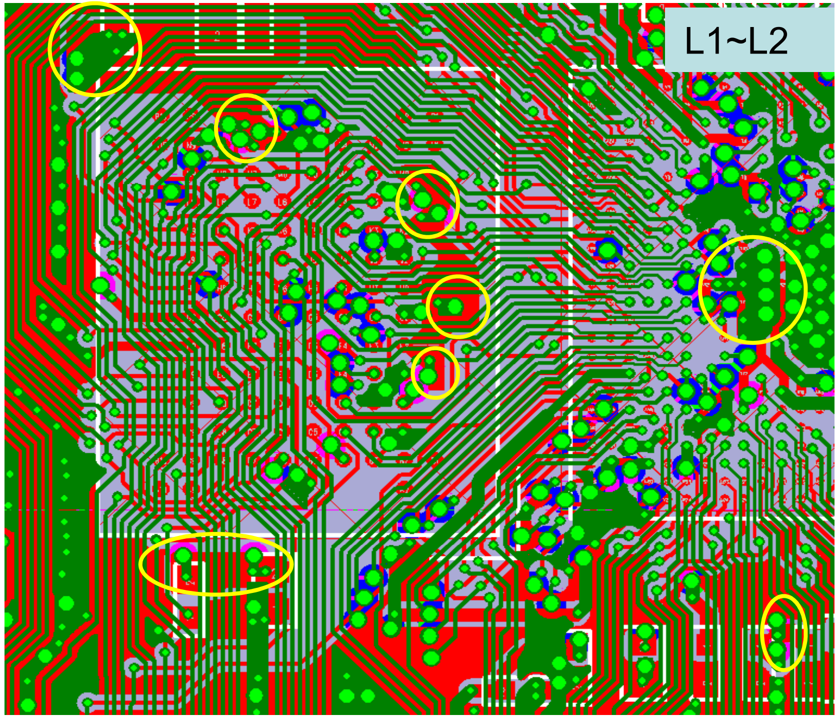
Vm Notice(1/2):

- Vm Via Quantity Suggestion:
  1. blind via(L1-L2): one via per one Vm ball or one de-cap if possible
  2. buried via(L2-L5): more is better (at least 3 via for BB Vm balls)
  3. Please refer to the reference phone layout as below





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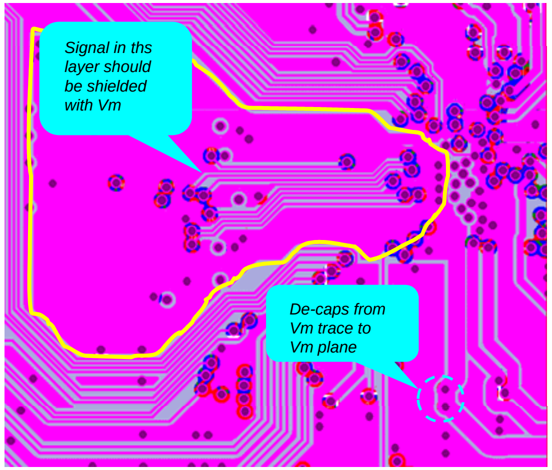
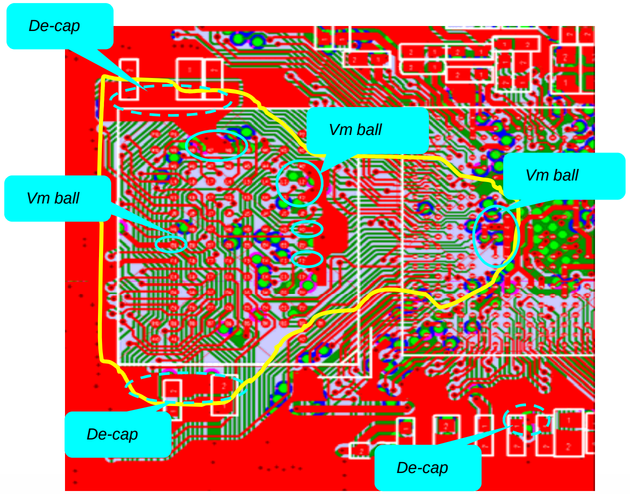
Vm Notice(2/2):

- Vm plane size suggestion:
  - 『 Method 1 』 : must cover all of BB & MCP Vm balls and should cover de-caps (close to Vm balls) if possible, see the two figure.
  - 『 Method 2 』: must cover the entire memory signal routes in signal layers, like 『 Method 1 』GND plane’s role.

『 Method 1 』





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High Speed Memory Layout

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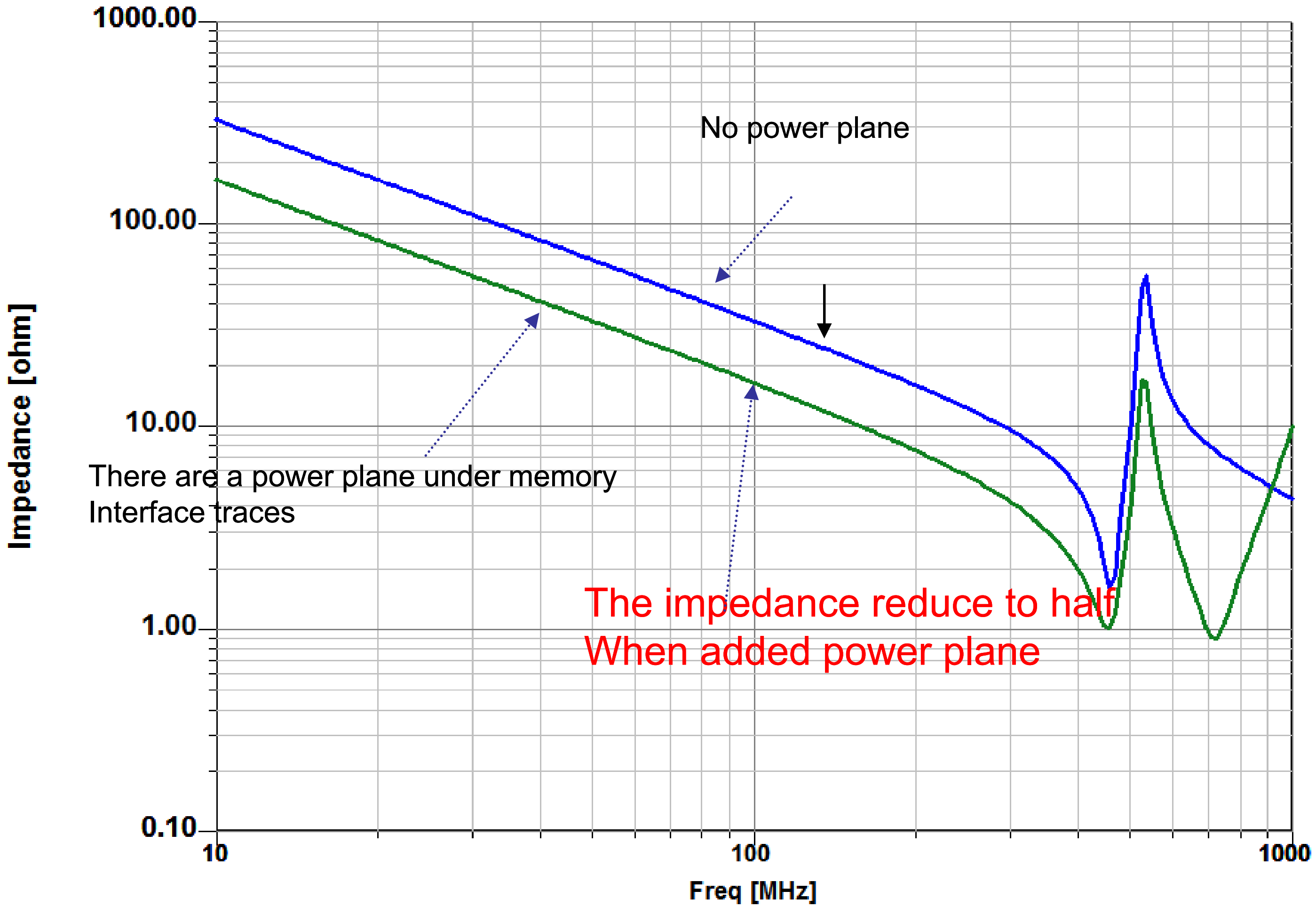
- If we take a good power plane under traces, we can get good trace impedance performance.



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High Speed Memory Layout

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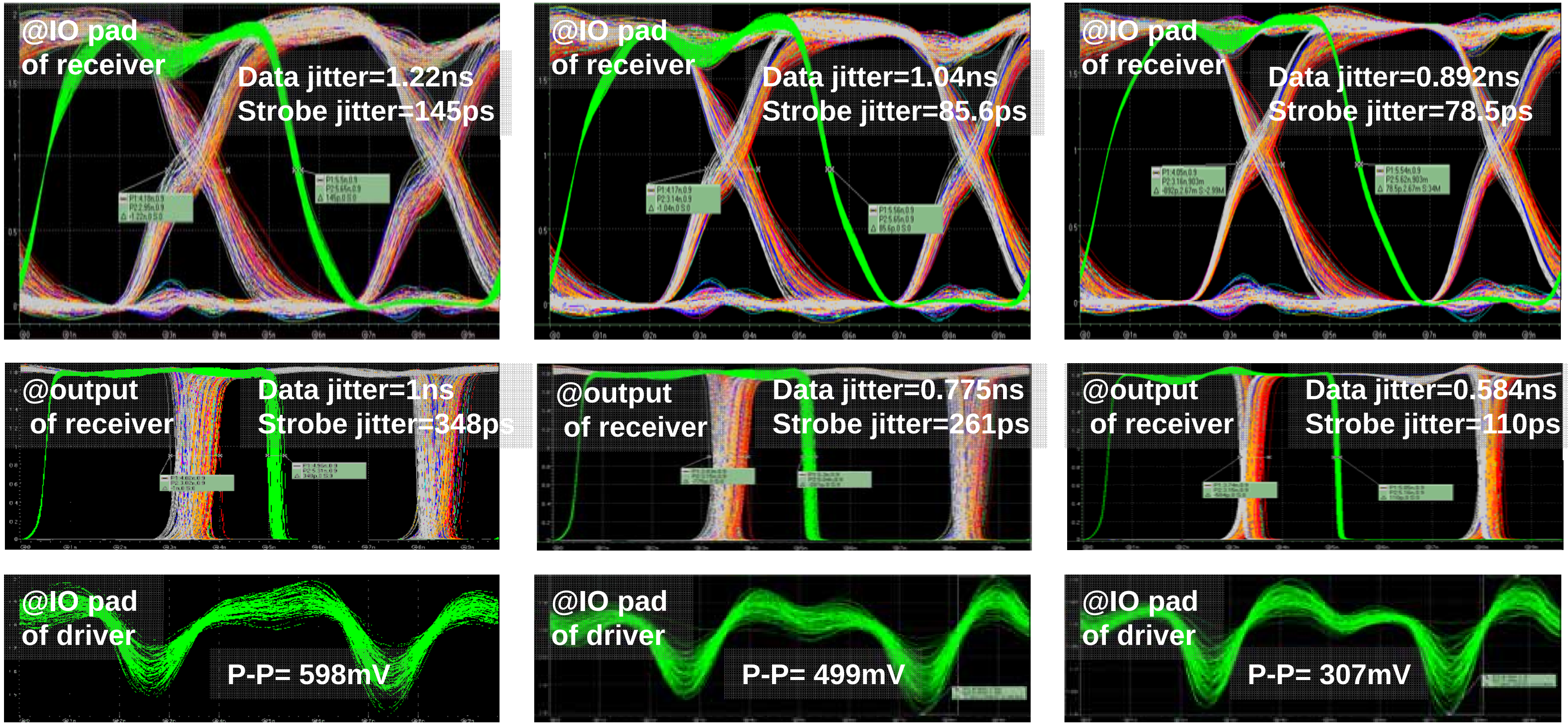
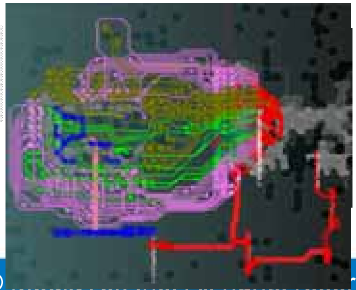
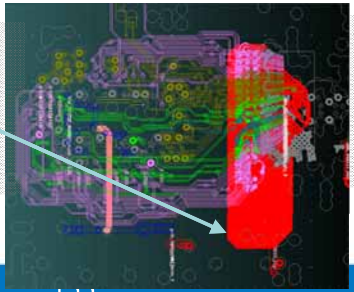
Add a power plane on PCB to enhance performance (reducing signal jitter)



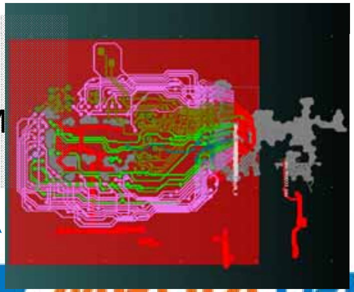
Only power trace
Bad



Added a small power plane under BB chip
Not good



Added power plane under BB chip and DRAM
Must



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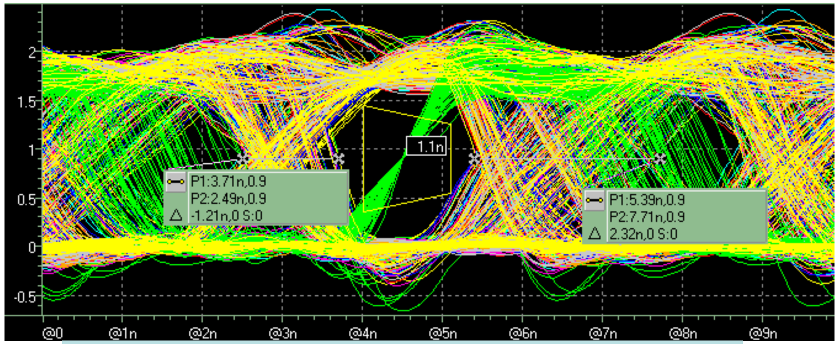
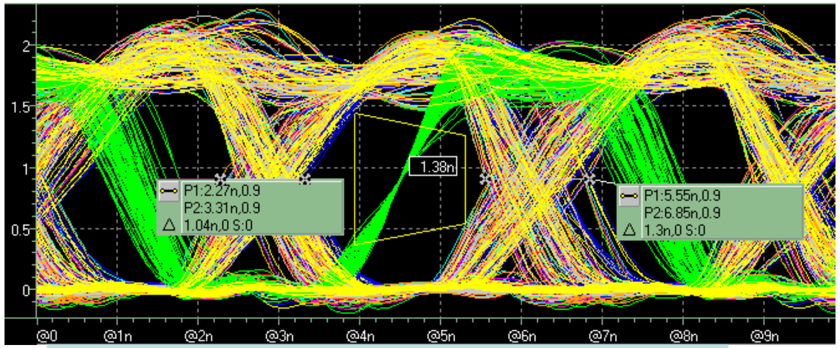
High Speed Memory Layout

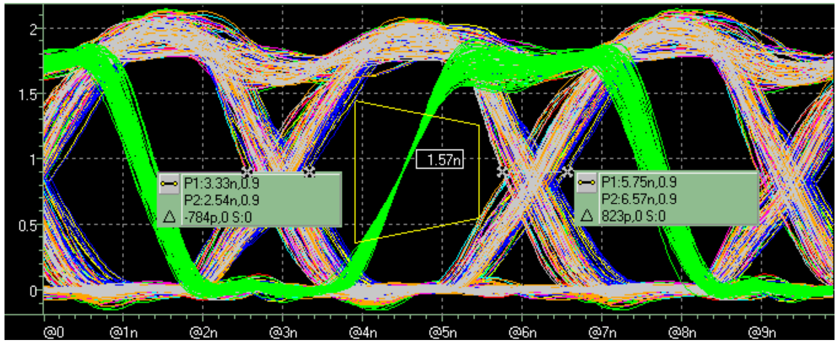
- Data eye simulation result



without power plane and short power trace from PMU



without power plane, but with short power trace from PMU



with power plane & short power trace from PMU

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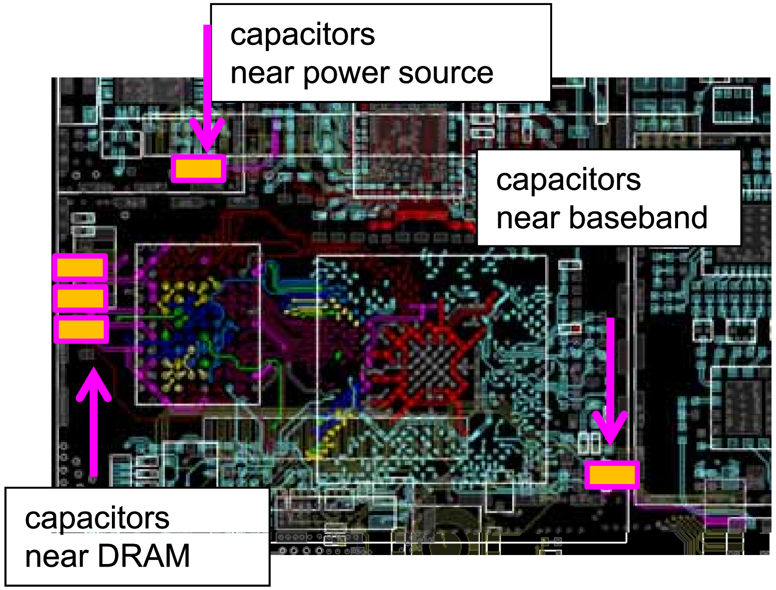
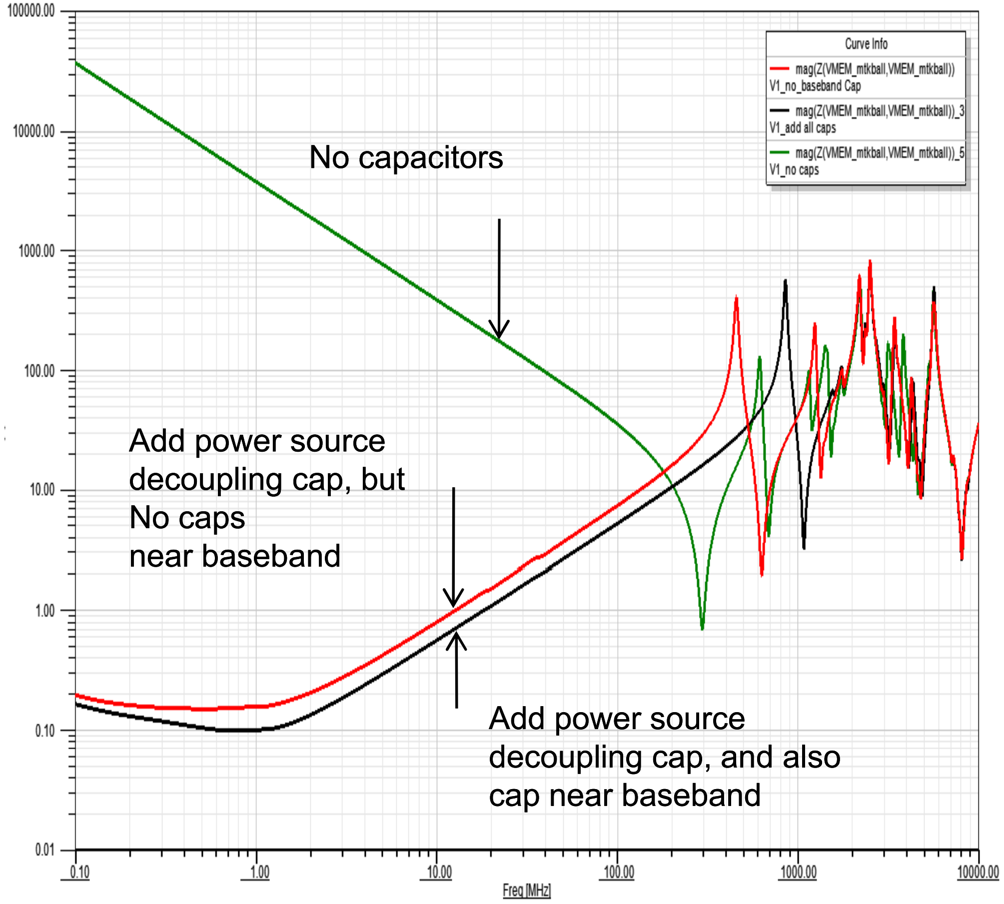
MT6516 Case study of Power Impedance (PDN)





- ***Decoupling capacitors near baseband are necessary*** for high speed mobile DRAM interface.
- ***The difference between the Impedance amplitude, will cause unstable DRAM operation. (In this case : "at -20℃ hang up")***
- Recommend to add decoupling capacitors near baseband & DRAM chip and power source.

→ Vm de-cap "near "IC is important!!

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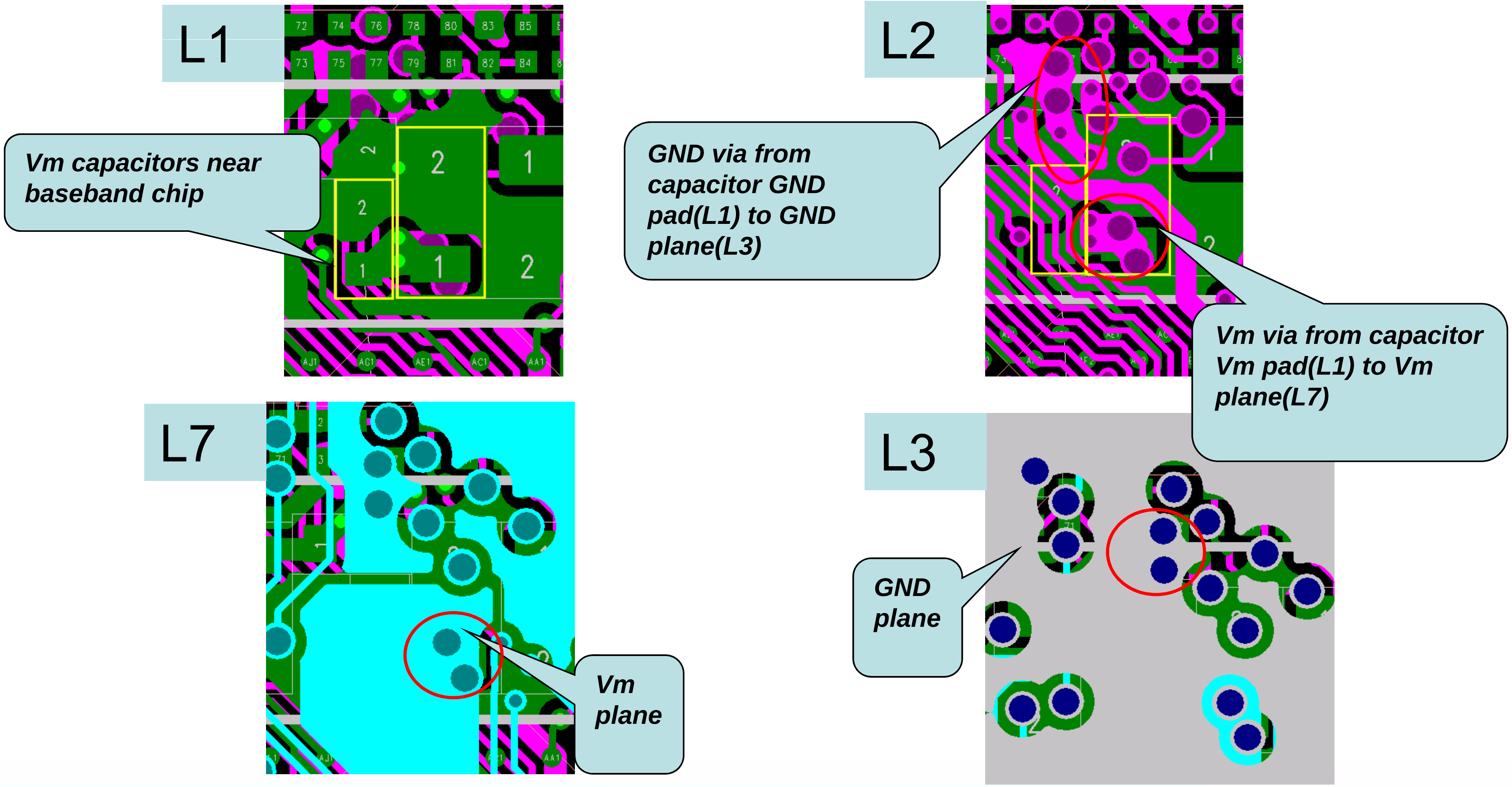
PDN Improvement (1): Vm de-cap via



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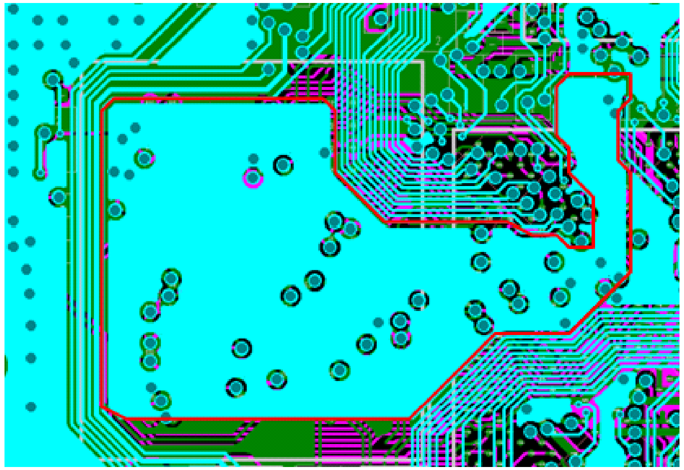
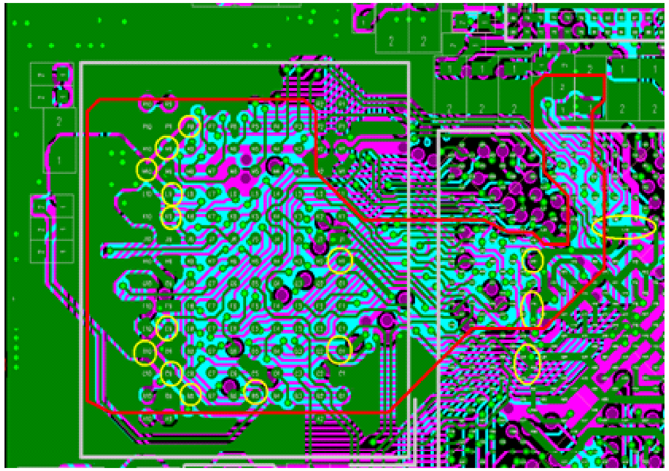
PDN Improvement (2): Vm plane size

- Please notice that the Vm plane size must be cover Vm balls of baseband chip and MCP as possible
  - ***if some Vm balls can't be covered by Vm plane, please check if the PDN of Vm trace/via between Vm plane to these Vm balls is optimally low. (try to move other trace and reserve space for Vm via)***
- Please notice that the via quantity between Vm plane to Vm balls, must follow the basic rule at least as above pages.





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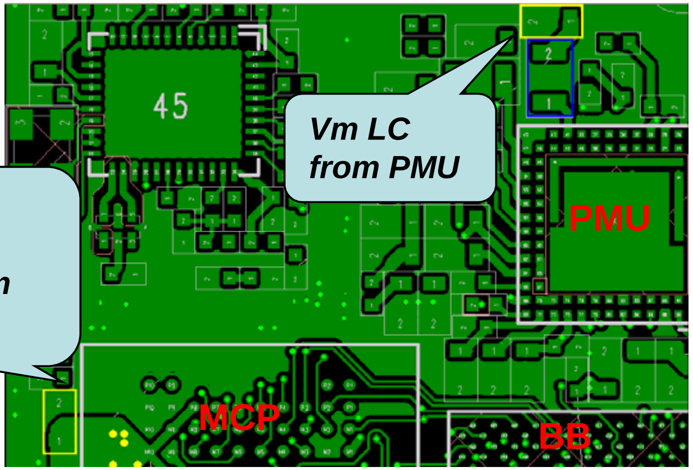
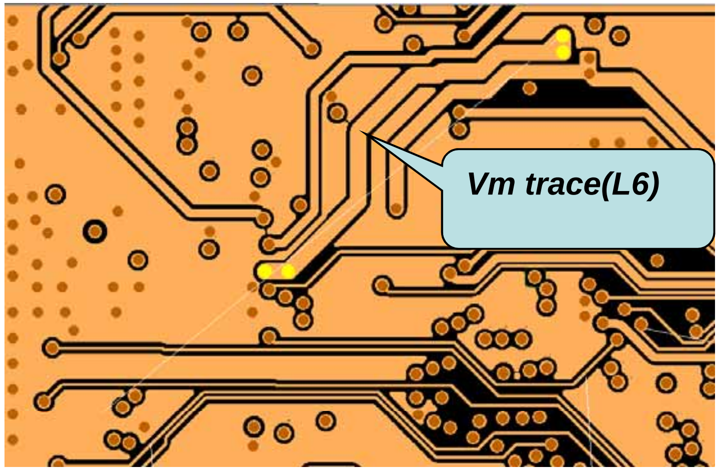
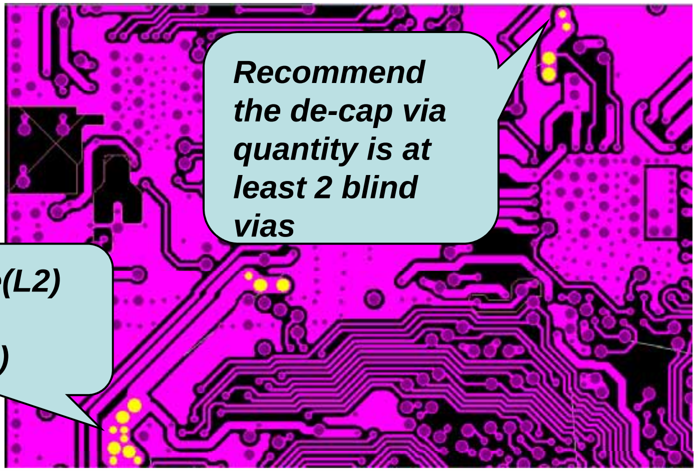
PDN Improvement (3): Vm trace/via







- Please notice that Vm via quantity is optimized (at least 2 buried via) when Vm trace from PMU to Vm plane changes layer no.

  Vm PDN: L1 LC→L6 trace→L2 trace →L7 Vm plane

- Please notice that the decoupling capacitor from Vm trace to Vm plane is needed.

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PDN comparison

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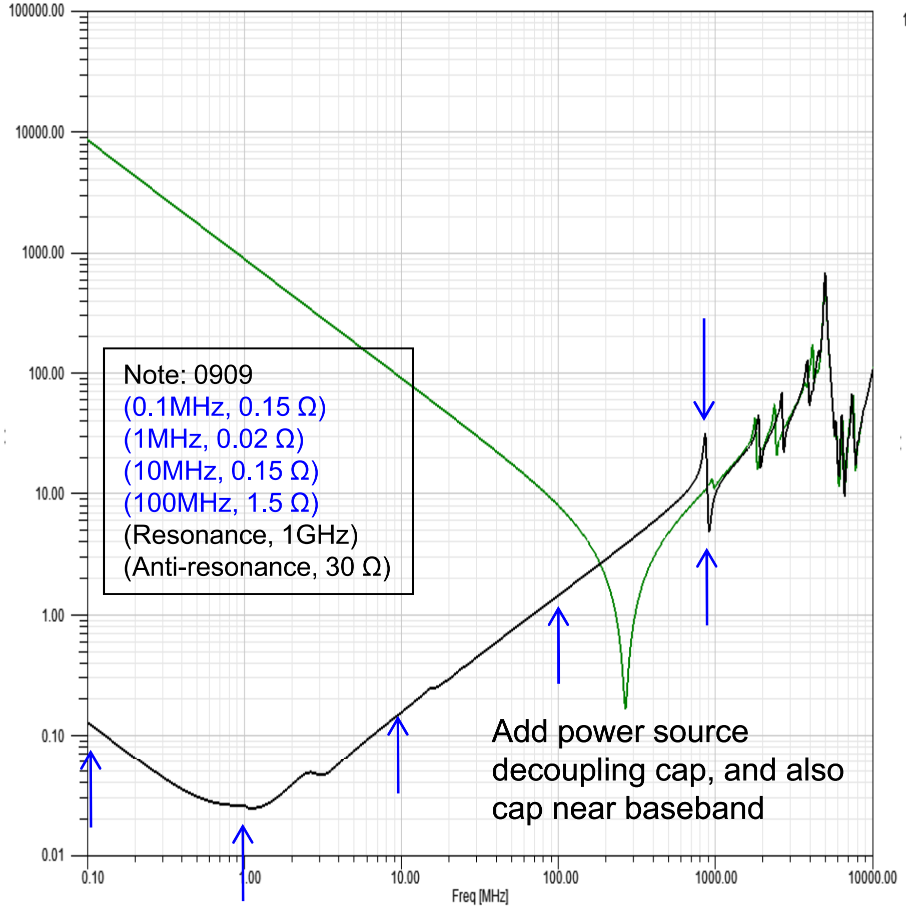
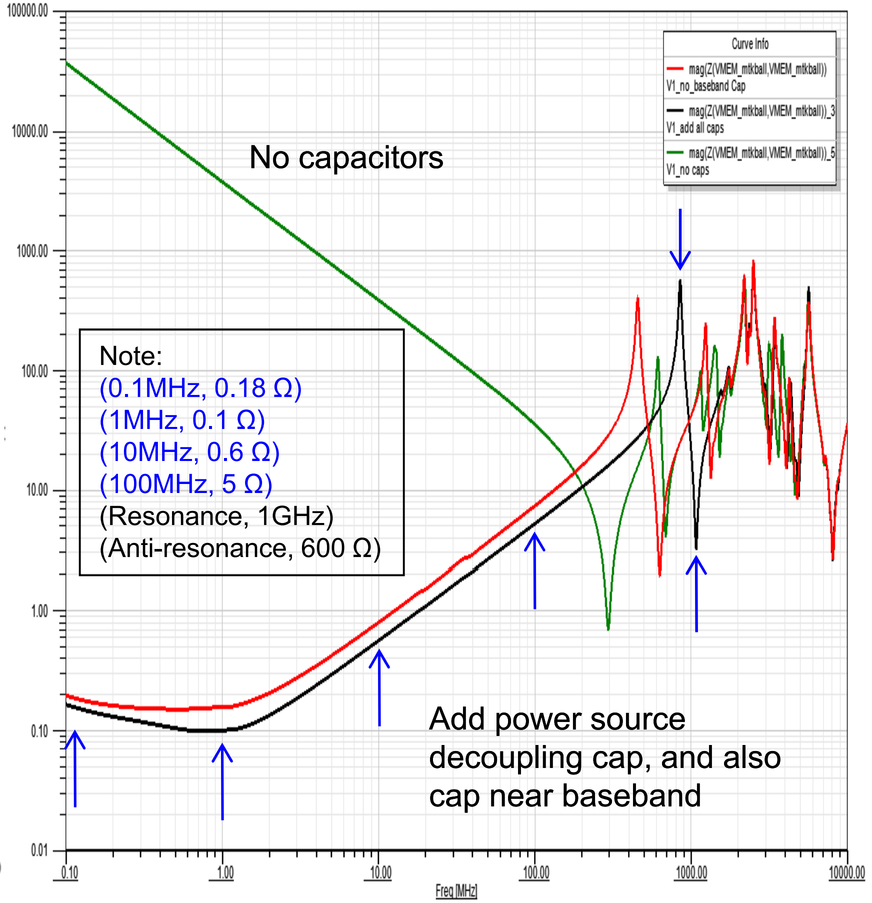
Improvement PDN (MTK in-house)



Customer's Board (Debug reference)



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PDN comparison table

	0.1 MHz	1 MHz	10 MHz	100 MHz	Resonance	Anti-resonance	Remark
MTK In-house (0909)	0.15 Ω	0.02 Ω	0.15 Ω	1.5 Ω	~1 GHz	30 Ω	(i) Improve power plane (ii) Improve power via
Customer's board	0.18 Ω	0.10 Ω	0.60 Ω	5.0 Ω	~1 GHz	600 Ω	

Note: 0909
(0.1MHz, 0.15 Ω)
(1MHz, 0.02 Ω)
(10MHz, 0.15 Ω)
(100MHz, 1.5 Ω)
(Resonance, 1GHz)
(Anti-resonance, 30 Ω)

Note: customer's
(0.1MHz, 0.18 Ω)
(1MHz, 0.1 Ω)
(10MHz, 0.6 Ω)
(100MHz, 5 Ω)
(Resonance, 1GHz)
(Anti-resonance, 600 Ω)

From simulation/experiment, we know that the small PDN impedance difference will cause unstable dram operation.

Therefore, we must lower the PDN impedance (from Vm source to BB/MCP Vm balls) as possible by following layout rule. That will let system become more robust.

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Suggested routing order (Signal layout)

- Layout routing order
  - Please route traces in the following sequence:
    1. Power/GND plane
    2. Data group
    3. Clock group
    4. Command/Address/Control groups
  - Because signal integrity (SI) is highly related to solid ground and power plane, data groups are operating at twice the clock frequency.

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Suggested routing order (Signal layout)

1. Data group (1/2)
   - DQx and DQS should be routed in a group and routed in the same layer and reduce via counts if possible.
     e.g.
     D[0:7] is aligned to DQS[0];
     D[8:15] is aligned to DQS[1].
     So, D[0:7] must be routed in a group with DQS[0],
     and D[8:15] must be routed in a group with DQS[1].

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask

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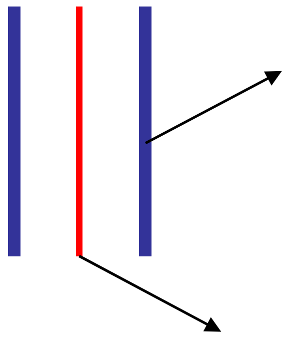
Suggested routing order (Signal layout)

1. Data group (2/2)
   - All different data group: (Max. trace length – 300 mil)< Trace length < (Max. trace length)

     | DQSx - Clock trace length | < 200 mil
   - To reduce the crosstalk on DQSx , GND shielding is required.



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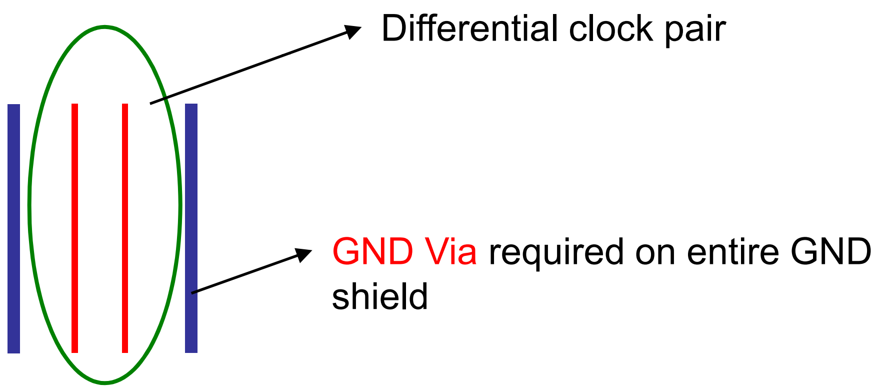
Suggested routing order (Signal layout)

2. Clock group

- Every trace must have solid power and ground plane near the entire route.
- Route these 2 clock traces in parallel and keep equal trace length.
- Within a clock pair:
  (Max. trace length – 50 mil) < Trace length < (Max. trace length),
  |DQS - Clock trace length| < 200 mil



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Suggested routing order (Signal layout)

3. Control/Command groups
   - Every trace must have solid power and ground plane near the entire route.
   - Within CMD/ADR group:
     |Max. (CMD/ADR trace length) – Min. (CMD/ADR trace length)| < 600 mil as possible

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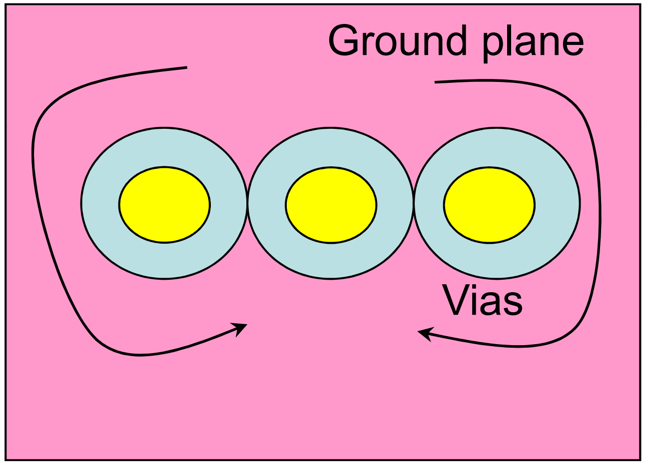
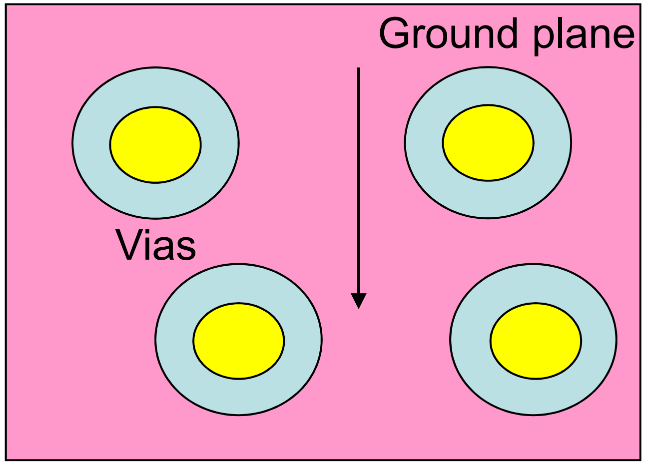
Other general layout considerations

- All bypass capacitors must be placed as close to the devices as possible, and GND of all capacitors should keep the shortest trace route to the GND plane.
- Avoid other sensitive traces near the memory traces.
- Separate traces even when they are on different layers.
- On the ground plane, do not block the ground return currents, as shown in the left figure.



Bad current return path



Good current return path

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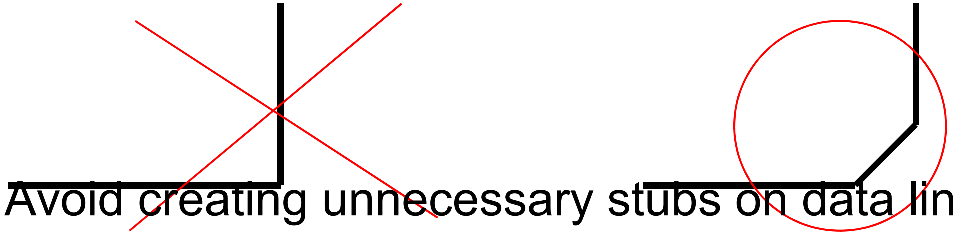
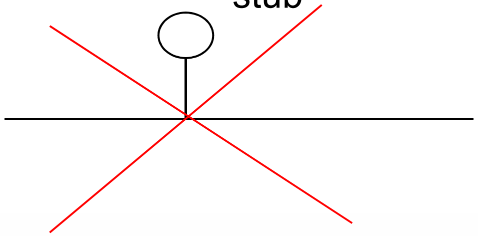
Other general layout considerations

– When it becomes necessary to turn 90°, make two 45° turns or an arc instead of making a single 90° turn. By making two 45° turns or an arc, it reduces reflections on the signals with impedance discontinuities minimized.



– Avoid creating unnecessary stubs on data lines, if a stub is unavoidable, please keep the stub as short as possible.



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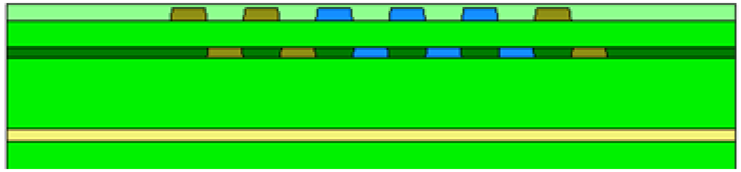
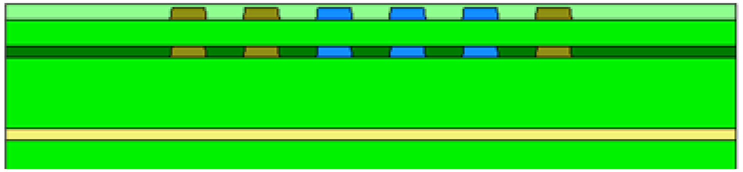
Other general layout considerations

– If two adjacent layers are signal layers, please avoid routing signal trace in Overlap method as the following picture.

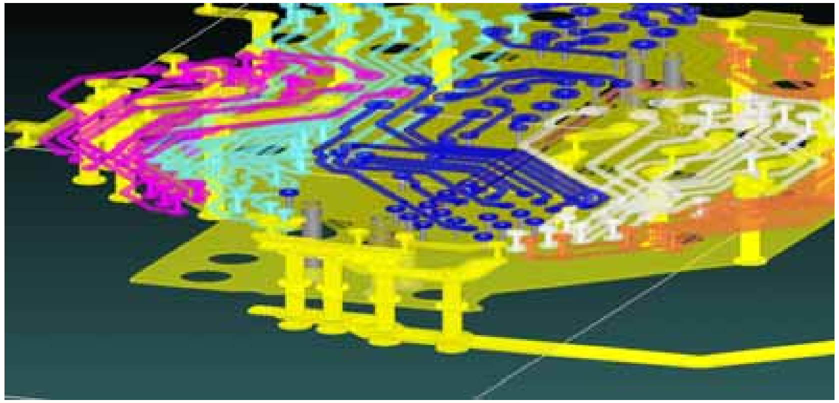


Interleave (O)



Overlap (X)

– Please check if the power via quantity(power plane to power pins) is optimized.



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Appendix :
MT5921 Application Note for MT6236

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Update History

2010.06.25

1. **Initial version**

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Outline

MT5921 Design Note

1. Signal Connection between MT5921 and MT6236
2. MT5921 NFI Bus Multi IO Usage
3. MT5921 Power Supply Plan for MT6236 Platform
4. MT5921 with BT Single Antenna Design

Appendix

1. CoB Qualified Vender List for Common Component (dual antenna)
2. Others Circuit Check Point (CoB design)

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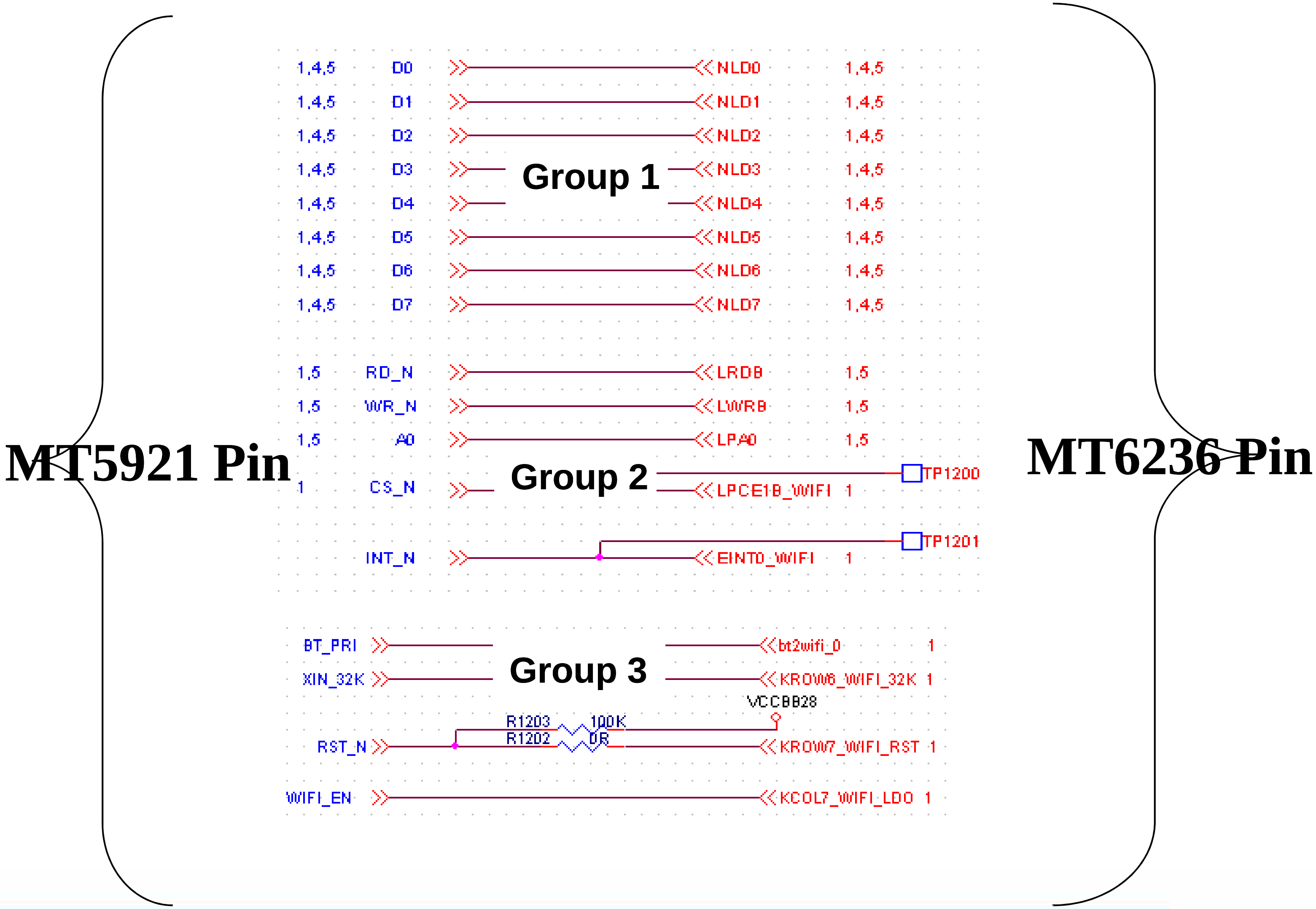
Connection between MT5921 and MT6236 (1/5)



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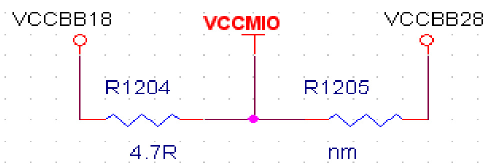
Connection between MT5921 and MT6236 (2/5)

- Group 1 : NFI interface (NLD0~7)
  - MT5921 shares NFI bus with NAND/LCM module so WiFi , NAND and LCM must have the same bus voltage domain.

MT5921 pin name	MT6236 pin name	Description
D0	NLD0	NFI , LCM and MT5921 should have the same NFI voltage domain setting.
D1	NLD1	
D2	NLD2	
D3	NLD3	
D4	NLD4	
D5	NLD5	
D6	NLD6	
D7	NLD7	

WiFi NFI IO voltage setting



For NFI=2V8, R1204=NC , R1205=4.7R

For NFI=1V8, R1204=4.7R , R1205=NC

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Connection between MT5921 and MT6236 (3/5)

– Group 2-1: LCM interface(NFI control signals)

MT5921 pin name	MT6236 pin name	Description
RD_N	LRDB	
WR_N	LWRB	
A0	LPA0	
CS_N	LPCE1B	

– Group 2-2: MT5921 interrupt signal

MT5921 pin name	MT6236 pin name	Description
INT_N	EINT0	**MUST connect WIFI EINT to MT6236 EINT0 !!** Because EINT0 power domain = DVDD_NFI EINT1~6 power domain = DVDD28 Only EINT0 meets MT5921 requirement.

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Connection between MT5921 and MT6236 (4/5)

– Group 3-1 : BT PTA connection

MT5921 pin name	MT6236 pin name	Description
BT_PRI	bt2wifi_0(GPIO64)	**WiFi BT co-existence signal**

– Goup3-2 : MT5921 32K digital slow clock signal

- MT5921 needs **+2.8V voltage domain 32kHz** signal.
- MT5921 **32K must be always on** even BB enters power-save mode . Please use MT6236 **CLK out function GPIO signals which belong to DVDD28/VIO power domain**.

MT5921 pin name	MT6236 pin name	Power domain
XIN_32K	GPIO17	DVDD_KP=VIO case
	GPIO 8/42/58/63	DVDD28
	GPIO 31/32/36	DVDD_NFI=2.8V case

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Connection between MT5921 and MT6236 (5/5)

- Goup3-3 : MT5921 RST_N and WIFI_EN signal
  - RST_N(+2.8V voltage domain) : WiFi power-on reset signal
  - WIFI_EN (+2.8V voltage domain) : WiFi external LDO(2.8V and 1.8V) control signal .
  - Please use GPIO signals which belong to DVDD28 power domain.
  - Suggest use GPIO signals with power-on PD function.

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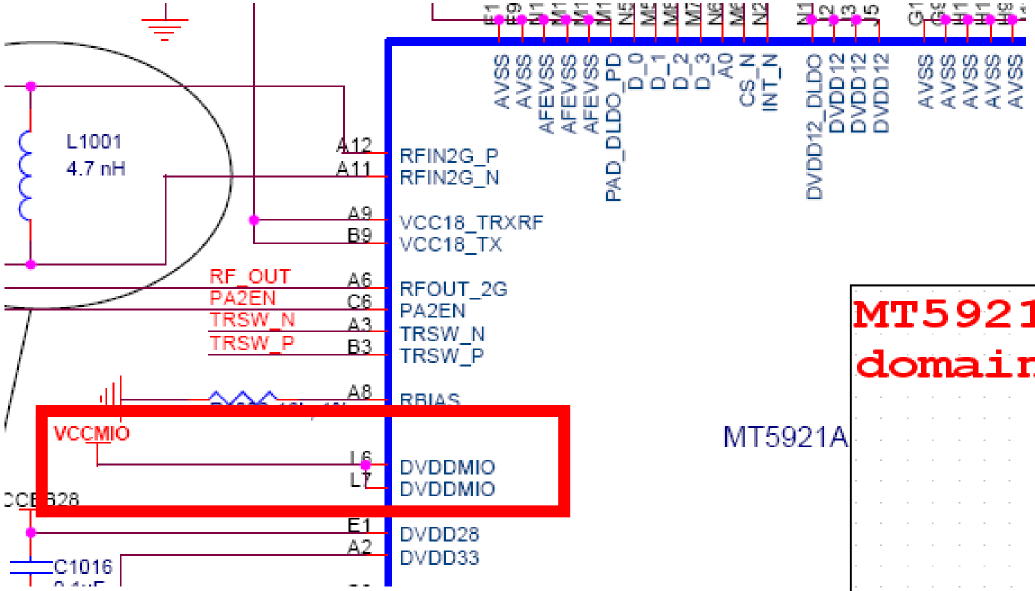
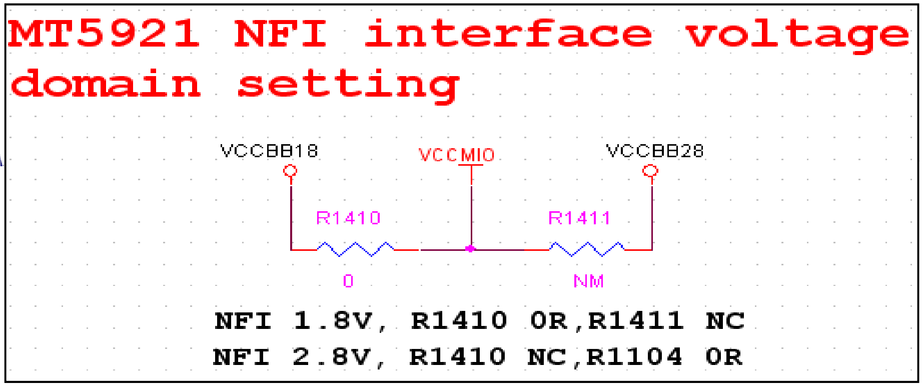
MT5921 NFI Bus Multi IO Usage (CoB)

- MT5921 supports +1.8V and +2.8V NFI bus
  - MT5921 NFI bus level selection depends on MT5921 VCCMIO power input.





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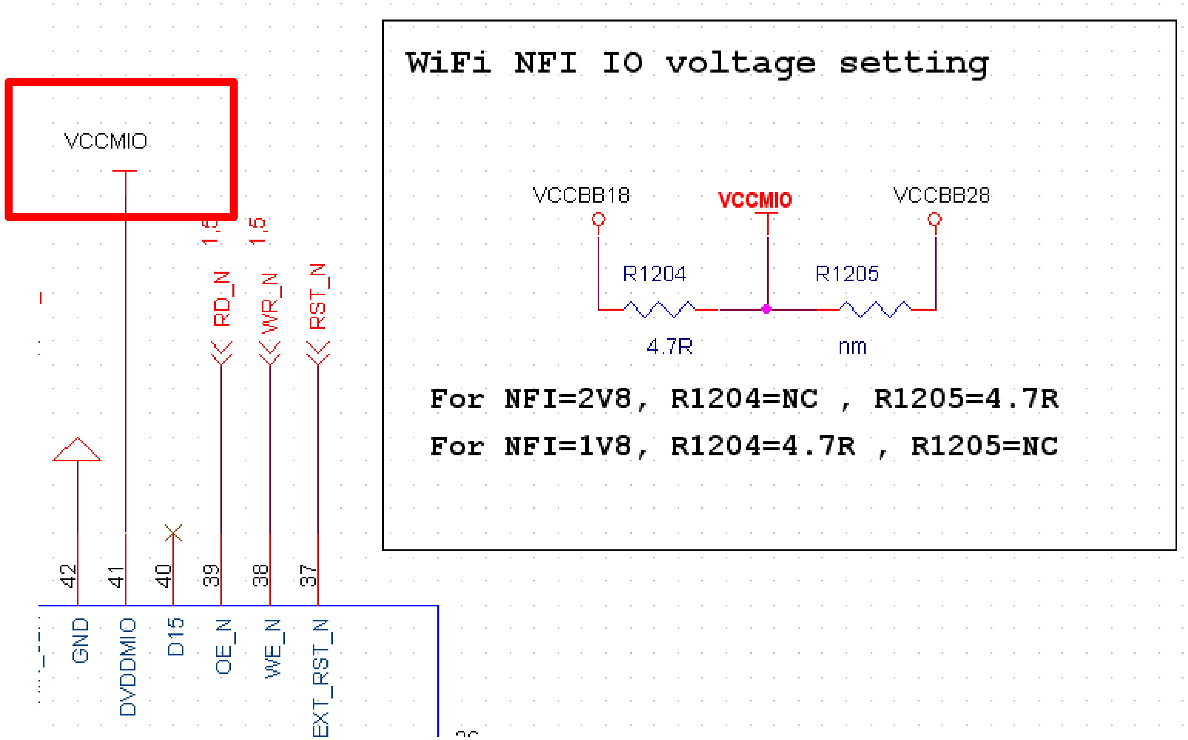
MT5921 NFI Bus Multi IO Usage (Module)

- MT5921 supports +1.8V and +2.8V NFI bus
  - MT5921 NFI bus level selection depends on MT5921 VCCMIO power input.



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MT5921 Power Supply at MT6236 Platform (1/4)

- Power-on sequence:
  - VDD18 power supply should be turned on first before DVDD28 power supply in order to avoid DVDD28 peak current.

- MT5921 power supply voltage and current requirement :

Power source	Description	Voltage range	Voltage tolerance	Peak current
MT5921 Power				
DVDDMIO	Digital IO power source	+1.8/+2.8V	+/-10%	<5mA
DVDD28/DVDD33	Digital IO power source	+2.8V	+/-10%	<5mA
VDD18	Analog power source	+1.8V	+/-0.1V	<150mA
External WiFi PA power				
VCC_PA	External PA power source	+3.3V	+/-10%	<170mA

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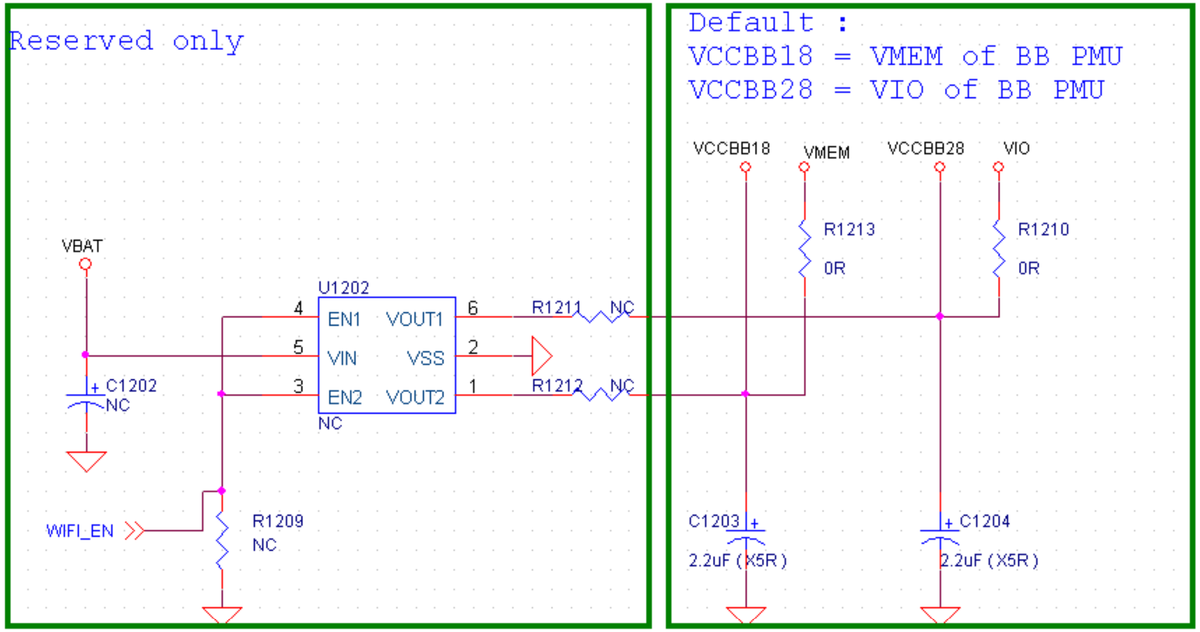
MT5921 Power Supply at MT6236 Platform (2/4)

- MT5921 +2.8V/+1.8V power supply plan at MT6236 platform:
- Solution A :
  - Share MT6236 PMU VMEM and VIO power ports with other devices.
- Solution B :
  - Use dedicated external +2.8V/+1.8V LDO component.



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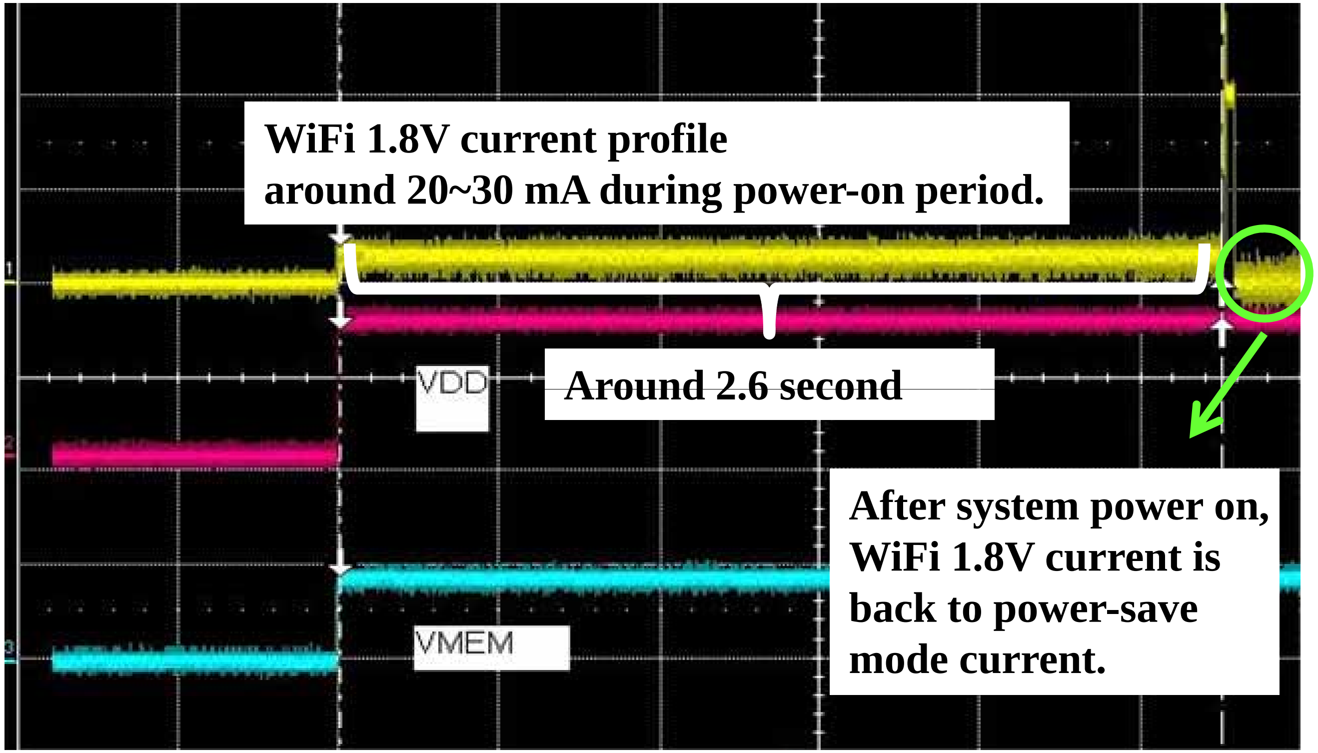
MT5921 Power Supply at MT6236 Platform (3/4)

– Note for power plan A :
  – Due to power sharing method, MT5921 +1.8V may cause some current leakage during system power-on period. After system completed power-on procedure and WiFi SW configure, MT5921 +1.8V current will return to power-save stage.



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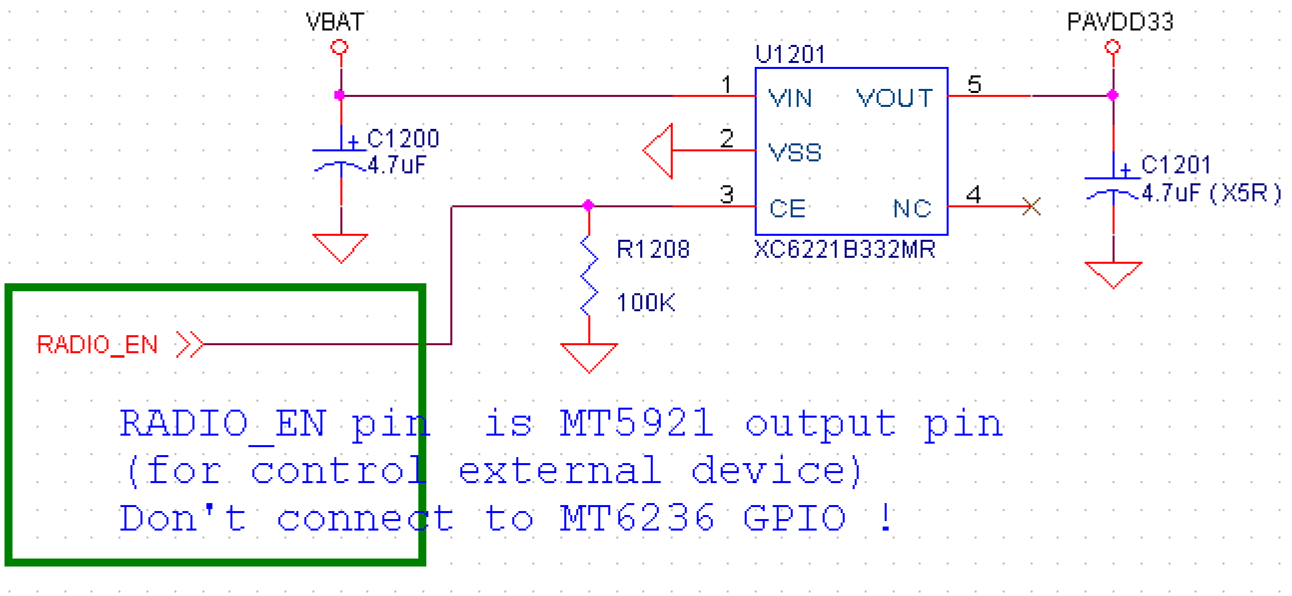
MT5921 Power Supply at MT6236 Platform (4/4)

- MT5921 external PA power supply plan at MT6236 platform:
  - Use MT5921 RADIO_EN pin to control WiFi PA LDO.



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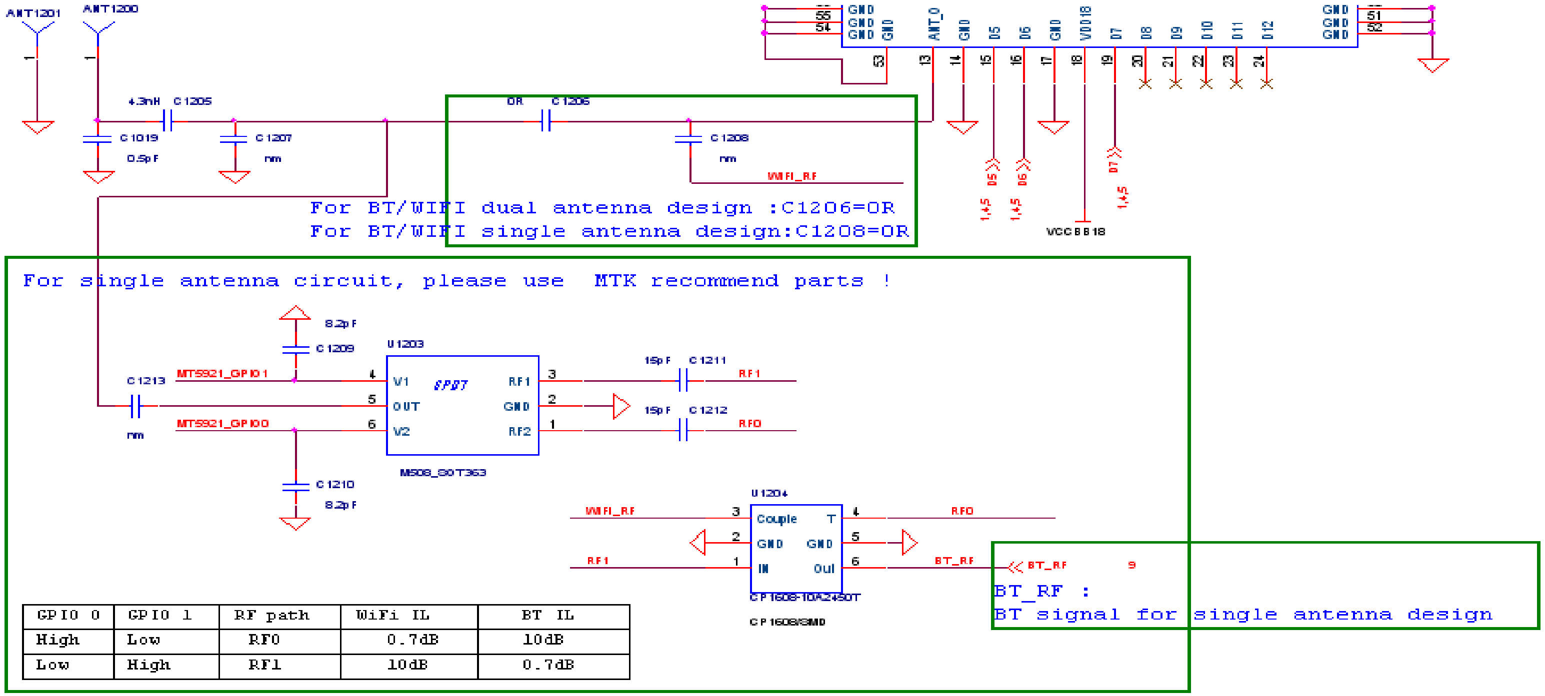
WiFi BT Single Antenna Design (1/5)

- WiFi SW uses MT5921 GPIO0 and GPIO1 hardware pin to control custom-mode SPDT to switch RF path between MT5921 and MT6236.
- Customers must use specific SW setting and HW component for single antenna design. **(Please ask PM to release SW/HW design package)**



GPIO 0	GPIO 1	RF path	WiFi IL	BT IL
High	Low	RF0	0.7dB	10dB
Low	High	RF1	10dB	0.7dB

WiFi BT Single Antenna Design (2/5)

– Single antenna component QVL :

Component	Part number	Package	Manufacturer	Note	MP date
*Switch	M508 (50ohm terminate.)	SOT-363	Hexwave	漢葳	Yes
	uPG2418TB(50ohm terminate.)		NEC	恩益禧	Yes
Coupler	CP1608-10A2450	1608	ACX	璟德	Yes
	LTC-1608-2G4S1		Mag.Layers	美磊	Yes

– *Switch is special 50 ohm terminated component.

– *Switch logic table:

ANT Path	MT5921 GPIO0	MT5921 GPIO1
Switch to WiFi	High	Low
Switch to BT	Low	High

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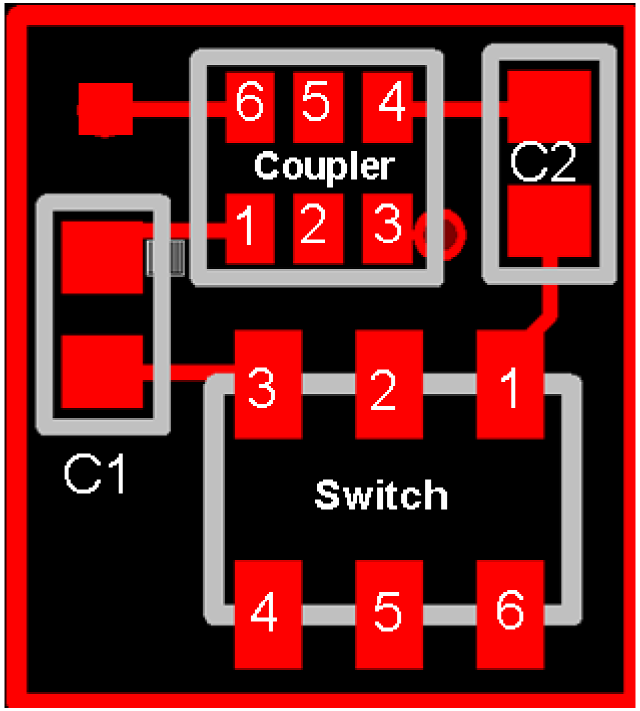
WiFi BT Single Antenna Design (3/5)



- PCB placement and layout notice :
  - RF trace between coupler and switch should be as short as possible.
  - All RF trace should keep 50 ohm impedance to maintain coupler RF characteristic, like isolation and so on.
  - Must 50 ohm well matching for switch antenna port and **antenna return loss < -12dB** in 2.4~2.5GHz frequency .
  - **Highly recommend using PIFA antenna design.** Other type antenna is not suitable and may cause single antenna performance degradation.

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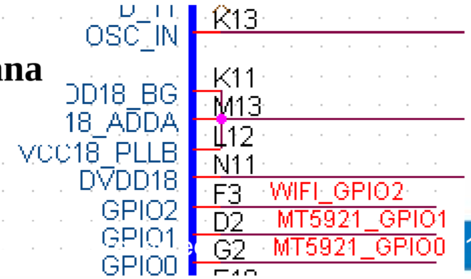
WiFi BT Single Antenna Design (4/5)

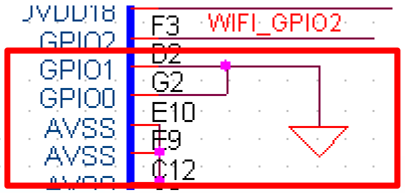
- Single antenna SW check notice :
  - Support branch : After W10.04 branch
    - For single and dual antenna design, SW library is different and customers need to maintain two set SW version for different HW design. Customers should prove the correct HW information for MTK SWPM in order to make sure MTK could provide the correct SW package.
    - Check SW make file setting for Single antenna design :
      - WIFI_BT_SINGLE_ANTENNA_SUPPORT = TRUE or FALSE
        TRUE for single antenna
        FALSE for dual antenna

–Single antenna SW will configure MT5921 GPIO 0/1 signal to output pin. Please don't apply single antenna SW on dual antenna HW design. It may cause 30~40mA current leakage due to MT5921 GPIO signal shortage to GND !

Correct single antenna GPIO design



Wrong GPIO design under single antenna SW



WiFi BT Single Antenna Design (5/5)

- ATE/META tool :
  - Support version : after W0952

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Appendix

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MT5921 CoB Qualified Vender List (1/3)

Component	Pin-to-Pin	Part Number	Package	Manufacturer	Lead Time	Vendor
Crystal	Yes	XTL571100-M118-043	3225	SIWARD	6 weeks	西華晶體
		7M40000014		TXC	6 weeks	台灣晶技
		TZ1596A		TAI-SAW	6 weeks	台灣嘉碩
		E3SB40.0000FAEE11M		HOSONIC	6 weeks	鴻星電子
		X3S040000BA1HZ-U		H.ELE	6 weeks	加高電子
		CXC3X400000GHVRB0M		Partron	3 weeks	三和科技
		XTL581100-M118-042	2520	SIWARD	6 weeks	西華晶體
		E2SB40.0000F10EE11M		HOSONIC	6 weeks	鴻星電子
		8Z40000055		TXC	3 weeks	台灣晶技
		EXS00A-CS02079		NDK	8 weeks	NDK
		TZ1478A		TAI-SAW	4 weeks	台灣嘉碩
		X2B040000L71HZ-U		H.ELE	6 weeks	加高電子
		CXC3X400000GJVRB0M		Partron	3 weeks	三和科技
RX Balun	Yes	BL1608-20B2450T	1608	ACX	6~8 weeks	璟德
		LDB182G4520C-110		Murata	4~6 weeks	台灣村田
		LTU-1608-2G4S1-A6		MAG.LAYERS	4~6 weeks	美磊
		RFBLN1608060AM1T59		WALSIN	2~4 weeks	華新

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MT5921 CoB Qualified Vender List (2/3)

Component	Pin-to-Pin	Part Number	Package	Manufacturer	Lead Time
Band Pass Filter	Yes	LFB212G45SG8A192	2012	Murata	4~6 weeks
		LTB-2012-2G4H6-A9		MAG.LAYERS	4~6 weeks
		CFL4111 514 17 2454K		YAGEO	4~6 weeks
		BF2012-L2R4DADT/LF		ACX	4~6 weeks
	Yes	BF1608-L2R4DAB	1608	ACX	6~8 weeks
		BF1608-L2R4DAD		ACX	6~8 weeks
		HMD950T		SOSHIN	4~6 weeks
		HMD952T		SOSHIN	4~6 weeks
		RFBPF1608060AM1T59		WALSIN	4~6 weeks
		LTB-1608-2G4H6-A4		MAG.LAYERS	4~6 weeks
		LTB-1608-2G4H6-A10		MAG.LAYERS	4~6 weeks
PA (Note 1)	Yes	12LP14E	2x2 mm QFN8	SST	4~6 weeks
		RTC6665 (w/ different matching value)		Richwave	1st: 8~12 weeks 2nd: 4~6 weeks
	No	RTC6640 (w/ different matching value)	1.5x1.5 mm DFN6	Richwave	1st: 8~12 weeks 2nd: 4~6 weeks

Note 1: For different PA designs, check the PA biasing circuits and follow the reference design. RTC6665 pin-out is the same with SST PA but **matching component value are different**, please contact with MTK for RTC6665 reference design.

MT5921 CoB Qualified Vender List (3/3)

Component	Pin-to-Pin	Part Number	Package	Manufacturer	Lead Time	Logic Table
SPDT Chip (Note 2)	No	uPG2030TK	1.5x1.1 mm minimold	NEC	8 weeks	Type 1 (reference design use)
	Yes	HWS408	2x2.2 mm SOT-363	Hexawave	4 weeks	
		HWS314				
		AS179-92LF	2x2.2 mm SC-70 6-lead	Skyworks	8 weeks	
	Yes	UPG2158T5K	1x1mm TSSON6	NEC	8 weeks	Type II
		Sky13323-378LF	1x1mm TSSON6	Skyworks	10 weeks	

Note 2: For MT5921, TRSW : TRSW_N signal table is as below:

TX mode: {TRSW=1,TRSW_N=0}

RX mode: {TRSW=0,TRSW_N=1}

For different SPDT chips (Type 1 or 2) , check the signal connection to avoid logic conflict.

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WiFi Module Qualified Vender List (1/2)

MT5921 Wi-Fi Module				
Vendor	Part Number	Size (mm)	Lead Time	Contact Window
USI	WM-G-MT-03	9 x 9 x 1.5	8 weeks	孫建文 (USI 代理商 益登科技) Mobile (China) : 86-139-0296-7212 (Taiwan): 886-0928-523-731 Office: 886-2-2657-8811 ext. 2504 audis@edom.com.tw 廖員續 (Taiwan) mariana@ms.usi.com.tw
Jorjin 佐臻	WG-2250	9 x 9 x 1.5	8 weeks	李傳勍(大陸代理商) Mobile: 86-13732663036 Office: 86-512-55191789 tiborlee@wdi-ks.com.cn 李明燉(Taiwan) Mobile : 886-939-527-168 Office: 886-2-2795-3660 ext.232 mtlee@jorjin.com.tw

All module pin out is pin to pin !!

(Module vendor could provide on-site SMD support)

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WiFi Module Qualified Vender List (2/2)

MT5921 Wi-Fi Module				
Vendor	**Part Number**	**Size (mm)**	**Lead Time**	**Contact Window**
群登	**S200**	**9 x 9 x 1.5**	**8 weeks**	**HT Chen (Taiwan)** **Mobile : 886-937-815-968** **Office: 886-3-3716-869 ext.210** **htchen@acsip.com.tw**

All module pin out is pin to pin !!

(Module vendor could provide on-site SMD support)

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Outline

MT5921 Design Note

1. Signal Connection between MT5921 and MT6236
2. MT5921 NFI Bus Multi IO Usage
3. MT5921 Power Supply Plan for MT6236 Platform
4. MT5921 with BT (MT6612/MT6616) Single Antenna Design

Appendix

1. Qualified Vender List for Common Component (dual antenna)
2. **Others circuit check point**

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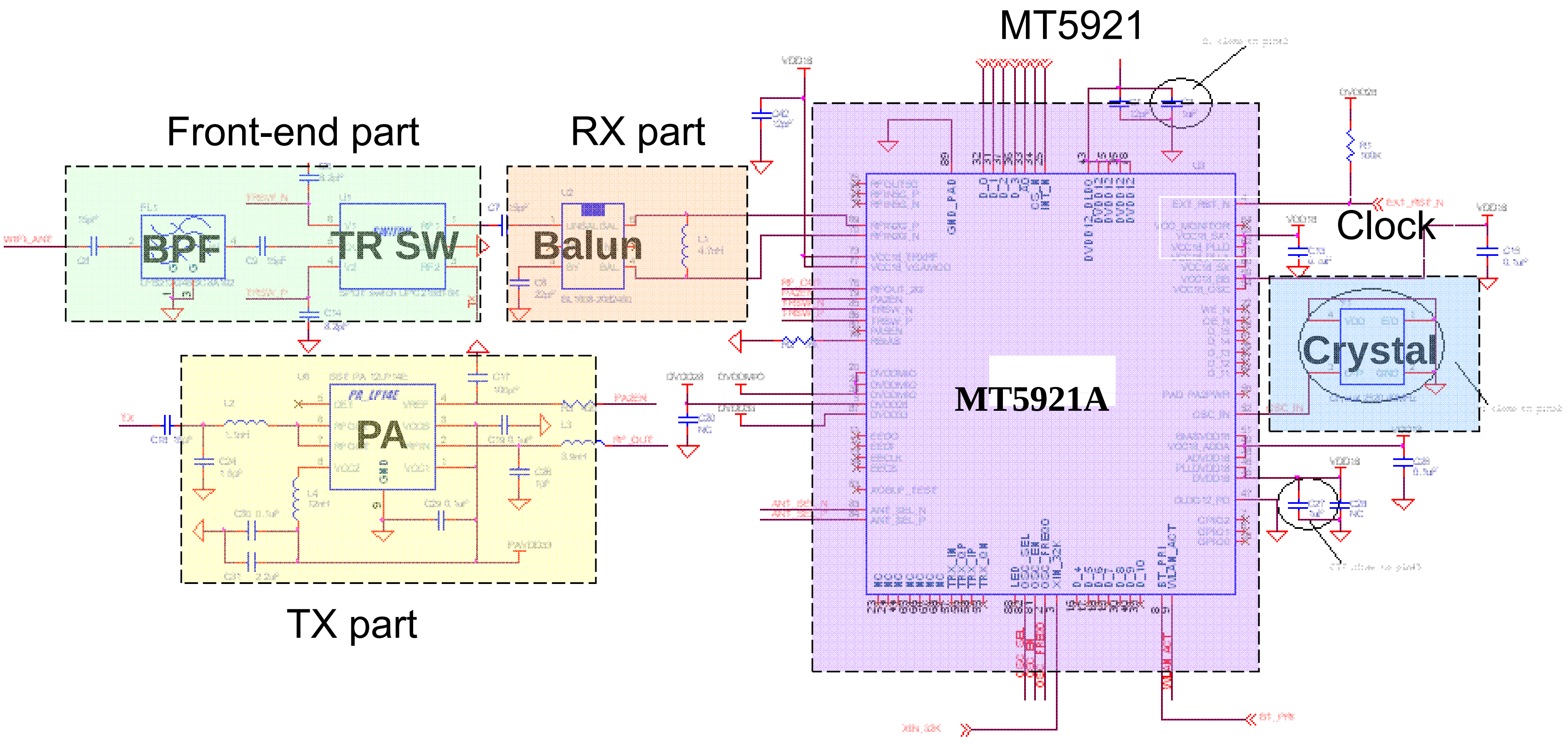
MT5921 CoB Reference Circuit (1/4)



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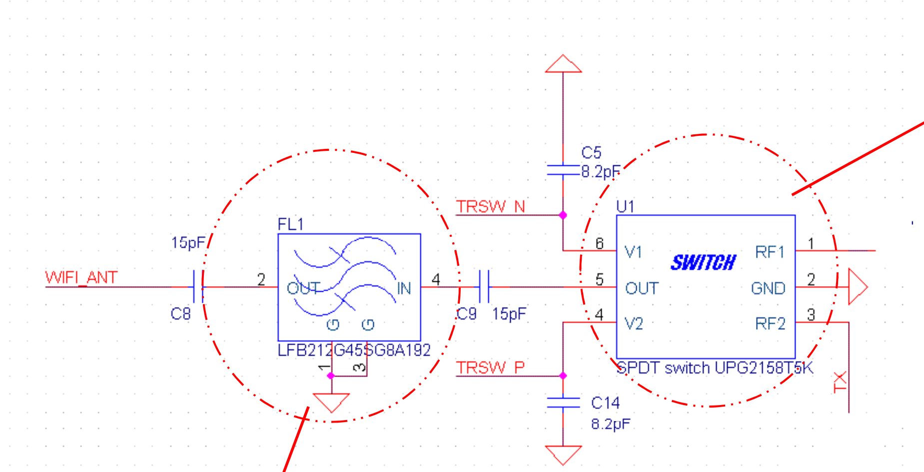
MT5921 CoB Reference Circuit (2/4)

RF Front-end part



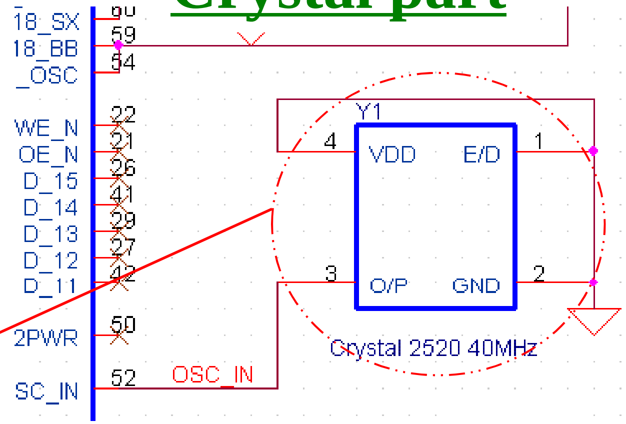
RF TX signal and RX signal path switch IC

For MT5921, TXRX mode signals only support below table setting:

	TRSW_P:	TRSW_N
TX mode:	1	0
RX mode:	0	1

High rejection band-pass filter for cellular-phone and WIFI co-existence

Crystal part



MT5921 could use OSC or crystal as system clock source

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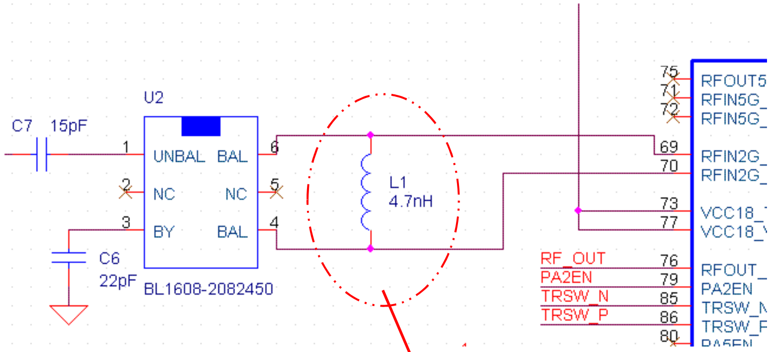
MT5921 CoB Reference Circuit (3/4)

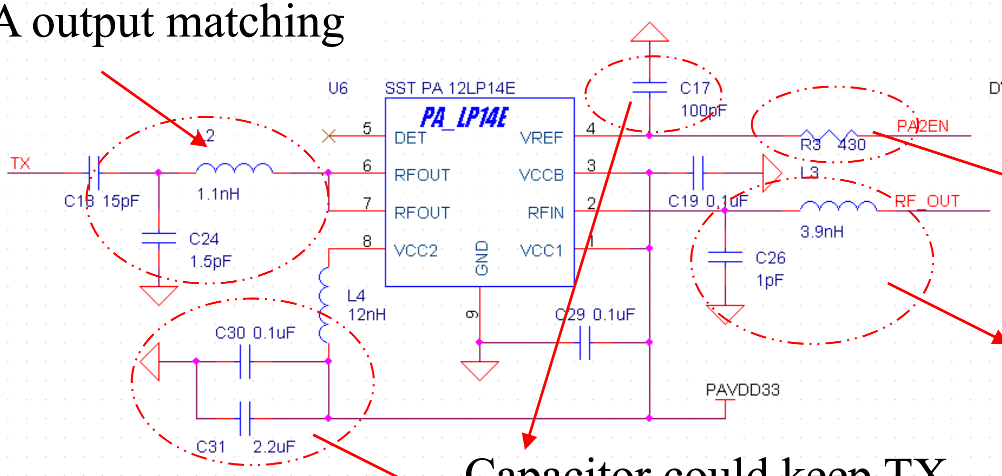
RF RX part



RF RX input matching

RF TX part

PA output matching



Use resistor to change PA bias voltage

RF TX output matching

Capacitor could keep TX performance stable

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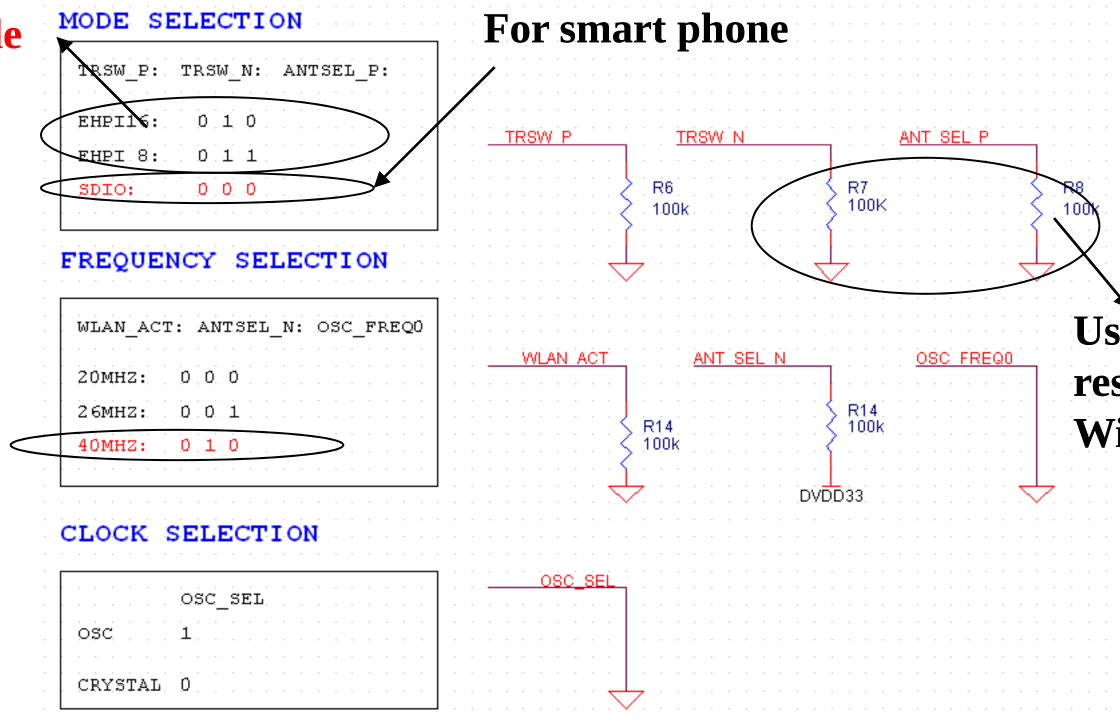
MT5921 CoB Reference Circuit (4/4)

For feature phone
Default is 8 bit mode

For smart phone



Use pull high or pull low resistors will depend on WiFi mode setting.

MT5921 uses strap-pin function to configure IC interface, clock frequency and clock type setting. These pins are input mode at power-on stage and return to other function in normal operation mode.
Please don't remove strap pin function 100K resistor !!!

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